JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH IN EMBEDDED SYSTEMS & VLSI DESIGN/VLSI AND EMBEDDED SYSTEMS/ ELECTRONICS DESIGN TECHNOLOGY.

EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Embedded System Design	25	75	4	0	0	4
PC-2	VLSI Technology	25	75	4	0	0	4
PC-3	CMOS Analog Integrated Circuit Design	25	75	4	0	0	4
PE-1	Hardware Software Co-Design Digital System Design Advanced Computer Architecture	25	75	**3**	0	0	3
PE-2	VLSI DSP Architectures CMOS Digital Integrated Circuit Design CPLD and FPGA Architectures and Applicat	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	VLSI Laboratory	25	75	0	0	3	2
Seminar I	Seminar - I	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Low Power VLSI Design	25	75	4	0	0	4
PC-5	CMOS Mixed Signal Circuit Design	25	75	4	0	0	4
PC-6	Real Time Operating Systems	25	75	4	0	0	4
PE-3	Advanced Digital Signal Processing System On Chip Architecture Embedded Networking	25	75	**3**	0	0	3
PE4	Design for Testability Physical Design Automation Scripting Languages	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Embedded Systems Laboratory	25	75	0	0	3	2
Seminar II	Seminar - II	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review II	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review III	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	100	0	0	0	16
Total	**100**	**100**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

 # For Project review I, please refer 7.10 in R17 Academic Regulations.

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LOW POWER VLSI DESIGN (PC - 4)

UNIT – I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT – III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT – IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT – V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits – Analysis and Design", TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

REFERENCE BOOKS:

1. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press
2. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press, /Wiley International, 1998.
3. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley, & Sons, 2000.
4. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
5. Bellamour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", A Kluwer Academic Press.
6. Siva G. Narendran, Anatha Chandrakasan, "Leakage in Nanometer CMOS Technologies", Springer, 2005.

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CMOS MIXED SIGNAL CIRCUIT DESIGN (PC - 5)

UNIT - I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT - II

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT - IV

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH Edition, 2002
2. Philip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, International 2nd Edition/Indian Edition, 2010.
3. David A. Johns,Ken Martin, “Analog Integrated Circuit Design”, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. Rudy Van De Plassche, “CMOS Integrated Analog-to- Digital and Digital-to-Analog converters”, Kluwer Academic Publishers, 2003
2. Richard Schreier, “Understanding Delta-Sigma Data converters”, Wiley Interscience, 2005.
3. R. Jacob Baker, “CMOS Mixed-Signal Circuit Design”, Wiley Interscience, 2009.

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REAL TIME OPERATING SYSTEMS (PC - 6)

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOK:

1. Qing Li, “Real Time Concepts for Embedded Systems”, Elsevier, 2011

REFERENCE BOOKS:

1. Rajkamal, “Embedded Systems- Architecture, Programming, and Design”, 2007, TMH.
2. W. Richard Stevens, Stephan A. Rago, “Advanced UNIX Programming”, 2006, 2nd Edition, Pearson.
3. Dr. Craig Hollabaugh, “Embedded Linux: Hardware, Software and Interfacing”, 2008, 1st Edition, Pearson.

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ADVANCED DIGITAL SIGNAL PROCESSING (PE - 3)

UNIT – I

Review of DFT, FFT, IIR Filters, and FIR Filters: Introduction to filter structures (IIR & FIR).Implementation of Digital Filters, specifically 2nd Order Narrow Band Filter and 1st Order All Pass Filter. Frequency sampling structures of FIR, Lattice structures, Forward prediction error, backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT - II

Non-Parametric Methods: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT - III

Parametric Methods: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

UNIT – IV

Multi Rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion. Examples of up-sampling using an All Pass Filter.

UNIT – V

Applications of Multi Rate Signal Processing: Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Sub-band Coding of Speech Signals, Quadrature Mirror Filters, Transmultiplexers, Over Sampling A/D and D/A Conversion.

TEXT BOOKS:

1. J. G. Proakis& D. G. Manolakis, “Digital Signal Processing: Principles, Algorithms & Applications”, 4th Ed., PHI.
2. Alan V Oppenheim & Ronald W Schaffer, “Discrete Time signal processing”, PHI.
3. Emmanuel C. Ifeacher, Barrie. W. Jervis, “DSP – A Practical Approach”, 2nd Edition., Pearson Education.

REFERENCE BOOKS:

1. S. M .Kay, “Modern spectral Estimation: Theory & Application”, 1988, PHI.
2. P.P.Vaidyanathan, “Multi Rate Systems and Filter Banks”, Pearson Education.
3. Kaluri V. Rangarao, Ranjan K. Mallik, “Digital Signal Processing: A Practitioner's Approach”, ISBN: 978-0-470-01769-2, 210 pages, November 2006 John Wiley.
4. S. Salivahanan, A. Vallavaraj, C. Gnanapriya, “Digital Signal Processing”, 2000,TMH

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SYSTEM ON CHIP ARCHITECTURE (PE - 3)

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, “Computer System Design System-on-Chip”, Wiley India Pvt. Ltd.
2. Steve Furber, “ARM System on Chip Architecture “, 2nd Edition, 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Ricardo Reis, “Design of System on a Chip: Devices and Components”, 1st Edition, 2004, Springer
2. Jason Andrews, “Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)”, Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, “System on Chip Verification – Methodologies and Techniques”, 2001, Kluwer Academic Publishers.

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EMBEDDED NETWORKING (PE - 3)

UNIT – I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Fire wire.

UNIT – II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT – III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT – IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT – V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1. Frank Vahid, Tony Givargis, “Embedded Systems Design: A Unified Hardware/Software Introduction”, John & Wiley Publications, 2002
2. Jan Axelson, “Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port”, Penram Publications, 1996.

REFERENCE BOOKS:

1. Dogan Ibrahim, “Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series”, Elsevier 2008.
2. Jan Axelson, “Embedded Ethernet and Internet Complete”, Penram publications, 2003.
3. Bhaskar Krishnamachari", “Networking Wireless Sensors”, Cambridge press 2005.

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DESIGN FOR TESTABILITY (PE - 4)

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, V. D. Agrawal, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M.A.Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
2. P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

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PHYSICAL DESIGN AUTOMATION (PE - 4)

UNIT – I

Introduction: Layout and design rules, materials for VLSI fabrication, basic algorithmic concepts for physical design, physical design processes and complexities.

Partition: Kernigham-Lin's algorithm, Fiduccia Mattheyes algorithm, Krishnamurthy extension, hMETIS algorithm, multilevel partition techniques.

UNIT – II

Floor-Planning: Hierarchical design, Wire length estimation, Slicing and non-slicing floor plan, polar graph representation, operator concept, Stockmeyer algorithm for floor planning, mixed integer linear program.

UNIT – III

Placement: Design types: ASICs, SoC, Microprocessor RLM; Placement techniques: Simulated annealing, Partition based, analytical, and Hall's quadratic; Timing and congestion considerations.

UNIT – IV

Routing: Detailed, global and specialized routing, channel ordering, channel routing problems and constraint graphs, routing algorithms, Yoshimura and Kuh's method, zone scanning and net merging, boundary terminal problem, minimum density spanning forest problem, topological routing, cluster graph representation.

UNIT – V

Sequential Logic Optimization and Cell Binding: State based optimization, state minimization, algorithms; Library binding and its algorithms, concurrent binding.

TEXT BOOKS:

1. Sarrafzadeh, M. and Wong, C.K, "An Introduction to VLSI Physical Design", 4th Edition, Mc Graw-Hill
2. Wolf. W, "Modern VLSI Design System on Silicon", 2nd Ed., Pearson Education.
3. Dreschler, "Evolutionary Algorithms for VLSI CAD", 3rd Edition, Springer.

REFERENCE BOOKS:

1. Sait, S.M, and Youssef, "VLSI Physical Design Automation: Theory and Practice", 1999, World Scientific Publishing Company.
2. Sherwani, "Algorithms for VLSI Physical Design Automation", 2nd Edition, Kluwer.
3. Lim, S.K, "Practical Problems in VLSI Physical Design Automation", Springer.

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SCRIPTING LANGUAGES (PE - 4)

UNIT - I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT - II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT - III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT - IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT – V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. David Barron, “The World of Scripting Languages”, Wiley Student Edition, 2010.
2. Brent Welch, Ken Jones and Jeff Hobbs., “Practical Programming in Tcl and Tk”, Fourth edition, Prentice Hall PTR.
3. Herbert Schildt, “Java the Complete Reference”, 7th Edition, TMH.

REFERENCE BOOKS:

1. Clif Flynt, “Tcl/Tk: A Developer's Guide”, 2003, Morgan Kaufmann Series.
2. John Ousterhout, “Tcl and the Tk Toolkit”, 2nd Edition, 2009, Kindel Edition.
3. Wojciech Kocjan and Piotr Beltowski, “Tcl 8.5 Network Programming book”, Packt Publishing.
4. Bert Wheeler, “Tcl/Tk 8.5 Programming Cookbook”, 2011, Packt Publishing Limited.

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EMBEDDED SYSTEMS LAB

Note: Minimum of 10 Experiments have to be conducted

Part-I

a. Write a program
   i. Write a simple program to print "hello world"
   ii. Write a simple program to show a delay.
   iii. Write a program for counting the number of times that a switch is pressed & released.
   iv. Write a c program to test loop time outs.
   v. Write a c program to test hardware based timeout loops.
   vi. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.
b. Write a program to create a portable hardware delay.
c. Write a loop application to copy values from P1 to P2
d. Develop a simple EOS showing traffic light sequencing.
e. Write a program to drive SEOS using Timer 0.

Part-II

The following programs are to be implemented on ARM Processor

1. Simple assembly program for addition, Subtraction, Multiplication, Division, Operating Modes, System Calls and Interrupts, Loops, Branches.
2. Write an Assembly program to configure and control general purpose input/output (GPIO) port pins
3. To read digital values from external peripherals and execute them with the target board
4. Program for reading and writing of a file
5. To demonstrate time delay program using built in timer / counter feature on IDE environment
6. To demonstrate a simple interrupt handler and setting up a timer
7. Program to demonstrate simple interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal
8. Program to interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment