JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS
EFFECTIVE FROM ACADEMIC YEAR 2019-20 ADMITTED BATCH

R19 COURSE STRUCTURE AND SYLLABUS

I YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - I	Digital Systems Design with PLDs	3	0	0	3
Professional Core - II	VLSI Technology and Design	3	0	0	3
Professional Elective - I	1. Embedded System Design 2. CMOS Analog Integrated Circuit Design 3. Advanced Microcontrollers	3	0	0	3
Professional Elective - II	1. Digital Signal Processors and Architectures 2. TCP/IP and ATM Networks 3. Advanced Data Communications	3	0	0	3
Lab - I	Digital System Design Lab	0	0	3	2
Lab - II	Scripting Languages Lab	0	0	3	2
	Research Methodology & IPR	2	0	0	2
Audit - I	Audit Course - I	2	0	0	0
	Total	**16**	**0**	**6**	**18**

I YEAR II – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - III	Advanced Computer Architecture	3	0	0	3
Professional Core - IV	Design of Fault Tolerant Systems	3	0	0	3
Professional Elective - III	1. System on Chip Architecture 2. Embedded Software Engineering 3. Embedded Real Time Operating Systems	3	0	0	3
Professional Elective - IV	1. Hardware and Software co-design 2. Low Power VLSI 3. Ad-hoc and Wireless Sensor Networks	3	0	0	3
Lab - III	Embedded Systems Lab	0	0	3	2
Lab - IV	Simulation Lab	0	0	3	2
	Mini project with Seminar	0	0	4	2
Audit - II	Audit Course - II	2	0	0	0
	Total	**14**	**0**	**10**	**18**

II YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Elective - V	1. Embedded Networks 2. Soft Computing Techniques 3. VLSI Signal Processing	3	0	0	3
Open Elective	Open Elective	3	0	0	3
Dissertation	Dissertation Work Review - II	0	0	12	6
	Total	**6**	**0**	**12**	**12**

II YEAR II - SEMESTER

Course Code	Course Title	L	T	P	Credits
Dissertation	Dissertation Work Review - III	0	0	12	6
Dissertation	Dissertation Viva-Voce	0	0	28	14
	Total	**0**	**0**	**40**	**20**

***For Dissertation Work Review - I, Please refer 7.8 in R19 Academic Regulations.**

Audit Course I & II:

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development Through Life Enlightenment Skills

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

DIGITAL SYSTEM DESIGN WITH PLDs (PC – I)

Pre-Requisite: Switching Theory and Logic Design

Course Objectives:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an overview of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

Course Outcomes:

1. To understands the minimization of Finite state machine.
2. To exposes the design approaches using ROM's, PAL's and PLA's.
3. To provide in depth understanding of Fault models.
4. To understands test pattern generation techniques for fault detection.
5. To design fault diagnosis in sequential circuits.
6. To provide exposure to various CPLDS and FPGAS available in market.
7. To acquire knowledge in one hot state machine design applicable to FPGA.
8. To get exposure to EDA tools.
9. To provide understanding in the design of flow using case studies.

UNIT-I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, virtex CLB and slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O standards, Additional features. [TEXTBOOK-1]

UNIT-II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. [TEXTBOOK-2]

UNIT-III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT-IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.1]

TEXTBOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Logic Design Theory-N.N.Biswas,PHI.

REFERENCES

1. Digital Circuits and Logic Design-Samuel C.LEE,PHI, 2008.
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

VLSI TECHNOLOGY AND DESIGN (PC – II)

Pre-requisite: Switching Theory And Logic Design

Course Objectives

1. Students from other engineering background to get familiarize with large scale integration technology.
2. To expose fabrication methods, layout and design rules.
3. Learn methods to improve Digital VLSI system's performance.
4. To know about VLSI Design constraints.
5. Visualize CMOS Digital Chip Design.

Course Outcomes

1. Review of FET fundamentals for VLSI design.
2. To acquires knowledge about stick diagrams and layouts.
3. Enable to design the subsystems based on VLSI concepts.

UNIT-I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT -II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT -III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT -IV

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT -V

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCES:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

EMBEDDED SYSTEMS DESIGN (PE – I)

Pre-Requisite: Microprocessor and Microcontrollers

Course Objectives

1. To differentiate between a General purpose and an Embedded System.
2. To provide knowledge on the building blocks of Embedded System.
3. To understand the requirement of Embedded firmware and its role in API.

Course Outcomes

1. Expected to differentiate the design requirements between General Purpose and Embedded Systems.
2. Expected to acquire the knowledge of firmware design principles.
3. Expected to understand the role of Real Time Operating System in Embedded Design.
4. To acquire the knowledge and experience of task level Communication in any Embedded System.

UNIT I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCES

1. Embedded Systems - Raj Kamal, TMH.

2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

CMOS ANALOG INTEGRATED CIRCUIT DESIGN (PE – I)

Pre-Requisite: Analog Electronics

Course Objectives: Analog circuits play a very crucial role in all electronic systems and due to continued iniaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes: After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT -I
MOS Devices and Modeling
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II
Analog CMOS Sub-Circuits
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III
CMOS Amplifiers
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV
CMOS Operational Amplifiers
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V
Comparators
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCES:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

ADVANCED MICROCONTROLLERS (PE - I)

Prerequisite: Microprocessors and Microcontrollers

Course Objectives:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes: After completing this course the student will be able to:

1. To explore the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Explore the ARM development towards the functional capabilities.
3. Expected to work with ASM level program using the instruction set.
4. Understand the architecture of ARM Cortex M and programming on it.

UNIT -I

ARM Embedded Systems:RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT -II

Introduction to the Arm Instruction Set : Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT -IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set,

Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT -V

Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXTBOOKS:

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, 3rd Ed.,

REFERENCES:

1. Arm System on Chip Architectures – Steve Furber, Edison Wesley, 2000.
2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES (PE - II)

Pre-Requisite: Digital Signal Processing

Course Objectives: The main objectives of the course are:

1. To provide a comprehensive understanding of various programs of Digital Signal Processors.
2. To distinguish between the architectural differences of ARM and DSPs along with floating point capabilities.
3. To explore architecture and functionality of various DSP Processors and can able to write programs.
4. To known about the connectivity of interfacing devices with processors.

Course Outcomes: Upon completing this course, the student will be able to:

1. Understand the various processing operations on Digital signals.
2. Know the architecture of DSP Processors TMS320C54XX, ADSP 2100, 2181 and Blackfin Processor.
3. Run the programs on DSP Processors.
4. Interface Memory and I/O devices with DSP Processors.

UNIT –I

Fundamentals of Digital Signal Processing: Digital signal-processing system, Sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and Interpolation, Computational Accuracy in DSP Implementations- Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II

Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III

Programmable Digital Signal Processors Commercial Digital Signal-Processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX Processors.

UNIT –IV

Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals

UNIT –V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications – J.G. Proakis & D.G. Manolakis, 4th Ed., PHI,2006.
2. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.

REFERENCES:

1. A Practical Approach to Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2009.
2. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, TMH, 2002.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al., S. Chand & Co. 2000.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

TCP/IP AND ATM NETWORKS (PE - II)

Prerequisite: Computer Networks

Course Objectives: The main objectives of the course are:

1. To study Network Layer Protocols, Next Generation IP protocols
2. To learn about User Datagram Protocol, Transmission Control Protocol and stream control Transmission protocol.
3. To understand techniques to improve QoS
4. To learn about Transport Layer Protocols for Ad Hoc Wireless Networks .
5. To study the features of ATM networks and various Interconnection Networks

Course Outcomes: At the end of the course, the student will be able to:

1. Get the concept of Network Layer Protocols and Transport Layer Protocols.
2. Understand and analyze about UDP, TCP AND SCTP protocols, flow and error control techniques.
3. Learn congestion control mechanisms and techniques to improve Quality of Service in switched networks
4. To understand the performance of TCP in Ad-hoc networks and various modified versions of TCP in ad-hoc networks
5. To understand features of Virtual circuit networks like ATM networks and their applications Design and analyze various types of Inter connection Networks.

UNIT-I

Network Layer: Network Layer Services**,** Packet switching**,** , Network Layer Performance, IPv4 Addresses, Internet protocol(IP), ICMP v4, IPv6 Addressing, IPv6 protocol, ICMPv6 protocol, Transition from IPv4to IPv6,Mobile IP

Forwarding of IP Packets, Delivery- Direct Versus Indirect Delivery, Forwarding- Forwarding Techniques, Forwarding Process, Routing Table, Unicast routing- Routing algorithms, Unicast routing protocols, Multicast routing, Multicasting basics.

UNIT -II

Transport Layer Introduction to Transport Layer, Transport layer services, Connectionless Versus Connection Oriented Protocols, Transport Layer Protocols: Simple Protocols, Stop and Wait Protocols, Go Back N Protocol, Selective Repeat Protocol, Bidirectional Protocols: Piggybacking Transport layer protocols Services and Port Numbers.

UDP, TCP and SCTP

User Datagram Protocol (UDP): User Datagram, UDP Services, UDP Applications

Transmission Control Protocol (TCP): TCP Services, TCP Features, Segments, TCP Connection, State Transition Diagram, Windows in TCP, Flow and Error Control, TCP Timers,

SCTP: SCTP Services, SCTP Features, Packet Format, An SCTP Association SCTP Flow and Error Control

UNIT III

Traditional TCP: Congestion Control, Additive Increase Multiplicative Decrease (AIMD), Slow Start, Fast recovery, fast retransmit

TCP in Wireless Domain: Traditional TCP, TCP over wireless**,** Snoop TCP , TCP-Unaware Link Layer Indirect TCP, Mobile TCP, Explicit Loss Notification, WTCP, TCP SACK , Transaction-Oriented TCP

Transport Layer Protocols for Ad Hoc Wireless Networks: TCP Over Ad Hoc Wireless Networks-Feedback-Based TCP, TCP with Explicit Link Failure Notification, TCP-Bus, Ad Hoc TCP, Split TCP.

UNIT IV

Congestion Control and Quality of Service: Quality of Service- Flow Characteristics, Flow Classes, Techniques to Improve QoS- Scheduling, Traffic Shaping, Resource Reservation, Admission Control, Integrated Services- Signaling, Flow Specification, Admission, Service Classes, RSVP, Problems with Integrated Services , Differentiated Services.

Queue Management: Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

UNIT V

ATM Networks: ATM-Design Goals, Problems, Architecture, Switching, ATM Layers

SONET/SDH: Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks

Interconnection Networks: Introduction, Banyan Networks, Properties, Crossbar switch, Three stage Class Networks, Rearrangeable Networks, Folding algorithm, Benes Networks, Lopping algorithm, Bit allocation algorithm.

TEXT BOOKS:

1. Data Communications and Networking - B. A.Forouzan, 5th edition, TMH, 2013.
2. Mobile Communications by Jochen H. Schiller, 2nd Edition, Pearson-Wesley, 2003.
3. Ad Hoc Wireless networks: Architectures and Protocols- C. Siva Ram Murthy and B. S.Manoj, PHI, 2004

REFERENCES:

1. ATM Fundamentals –N.N Biswas, Adventure Books,1998
2. Data Communications and Computer Networks - Prakash C. Gupta, PHI, 2006.
3. Data and Computer Communications - William Stallings, 8th ed., PHI, 2007.

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M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

ADVANCED DATA COMMUNICATIONS (PE - II)

Prerequisite: Digital Communication

Course Objectives: The main objectives of the course are:

1. To learn about basics of Data Communication networks, different protocols, standards and layering concepts.
2. To study about error detection and correction techniques.
3. To know about link layer, point to point, Medium Access and Control sub layer protocols.
4. To know about Switching circuits, Multiplexing and Spectrum Spreading techniques for data transmission.

Course Outcomes: At the end of the course, the student will be able to:

1. Understand the concepts of Networks and data link layer.
2. Acquire the knowledge of error detection, forward and reverse error correction techniques.
3. Compare the performance of different MAC protocols like Aloha, CSMA, CSMA/CA, TDMA, FDMA & CDMA.
4. Understand the significance of Switching circuits and characteristics of Wired LANs

UNIT -I

Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface.
Data Link Layer: Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

UNIT -II

Error Detection and Correction: Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks, Error Correction, Error correction single bit, Hamming code.
Cyclic Codes Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum
Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol

UNIT -III

Media Access Control (MAC) Sub Layer: Random Access, ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA),Controlled Access- Reservation, Polling- Token Passing, Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).
Wired LANS: Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet

UNIT-IV

Switching: Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch
Multiplexing: Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing.

Spectrum Spreading: Spread Spectrum-Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum
Connecting devices: Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.

UNIT V
Networks Layer: Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.
Unicast Routing: Introduction, Routing Algorithms-Distance Vector Routing, Link State Routing, Path Vector Routing, Unicast Routing Protocols- Routing Information Protocol(RIP), Open Short Path First .

TEXT BOOKS
1. Data Communications and Networking - B. A. Forouzan, 5th Ed., TMH, 2013.
2. Data and Computer Communications - William Stallings, 8th Ed., PHI, 2007.

REFERENCES
1. Data Communications and Computer Networks - Prakash C. Gupta, PHI, 2006.
2. Data Communications and Networking - B. A. Forouzan, 2nd Ed., TMH, 2013.
3. Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2008.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

DIGITAL SYSTEM DESIGN LAB (Lab – I)

Part –I:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in
13. Serial out and Parallel in Parallel Out.
14. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
15. Design of 4- Bit Multiplier, Divider.
16. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
17. Multiplication, and Division.
18. Design of Finite State Machine.
19. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

Part –II:

1. Static and Dynamic Characteristics of CMOS Inverter
2. Implementation of EX-OR gate using complementary CMOS, Psedo-NMOS, Dynamic and domino logic style
3. Implementation of Full Adder using Transmission Gates

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

SCRIPTING LANGUAGES LAB (Lab – II)

Prerequisites: Students should install Python on Linux platform.

List of Programs:

Part: I
Preliminary Exercises:

1. To demonstrate different number data types in Python.
2. To perform different Arithmetic Operations on numbers in Python.
3. To create, concatenate and print a string and accessing sub-string from a given string.
4. Write a python script to print the current date in the following format “Sun May 29 02:26:23 IST 2017”
5. To demonstrate working with dictionaries in python.
6. To find largest of three numbers.
7. Write a Python program to construct the a pattern, using a nested for loop.
8. Write a Python script that prints prime numbers less than 20.
9. To convert temperatures to and from Celsius, Fahrenheit.

Part: II:

10. To create, append, and remove lists in python.
11. To demonstrate working with tuples in python.
12. To find factorial of a number using Recursion.
13. Write a Python class to implement pow(x, n)
14. Write a script named copyfile.py. This script should prompt the user for the names of two text files. The contents of the first file should be input and written to the second file.
15. Write a program that inputs a text file. The program should print all of the unique words in the file in alphabetical order.
16. Write a Python class to find the frequency of each alphabet (of any language) in the given text document.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

RESEARCH METHODOLOGY AND IPR

Prerequisite: None

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information

and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students’”
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”

REFERENCES:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

ADVANCED COMPUTER ARCHITECTURE (PC – III)

Pre-Requisite: Computer Organization and Operating Systems.

Course Objectives:

- Explains instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
- Explains different classifications of instruction set architectures.
- Explains the advanced concepts such as instruction level parallelism, , out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.
- Examine software support for ILP, including VLIW and similar approaches.
- Teach memory hierarchy design issues, including caching and virtual memory approaches.
- Explains multiprocessor and parallel processing architectures.
- Gives the organization and design of contemporary processor architectures.
- As the current trend in computer architecture is towards chip-multiprocessing, the architecture of shared memory multiprocessors and chip level interconnect (network-on-chip) will be covered as future scope.

Course Outcomes: A student who has met the objectives of the course will be able to

- Understand advanced computer architecture aspects.
- Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures.
- Understand the architecture and limitations of chip-multiprocessing.
- Explain in detail about time-predictable computer architecture.
- Understand the operation of modern CPUs including pipelining, memory systems and busses.
- Design and emulate a single cycle or pipelined CPU by given specifications using Hardware Description Language (HDL).
- Write reports and make presentations of computer architecture projects.

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT -IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT -V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCES:

1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill.,
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk ,Pearson Ed.,

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

DESIGN OF FAULT TOLERANT SYSTEMS (PC – IV)

Pre-Requisite: Digital System Design with PLDs

Course Objectives:

- To provide broad understanding of fault diagnosis and tolerant design approach.
- To illustrate the framework of test pattern generation using semi and full automatic approach.

Course Outcomes:

- To acquire the knowledge of fundamental concepts in fault tolerant design.
- To acquire the knowledge of design requirements of self check-in circuits.
- To acquire the knowledge of test pattern generation using LFSR.
- To acquire the knowledge of design for testability rules and techniques for combinational circuits.
- To acquire the knowledge of scan architectures.
- To acquire the knowledge of design of built-in-self test.

UNIT - I

Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.
Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT - II

Self Checking circuits & Fail safe Design: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
Fail Safe Design- Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT - III

Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.
Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT - IV

Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket (RTS), LSSD On-chip self test, Self –

testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT - V

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXTBOOKS:

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala,PHI, 1984.
2. Digital System Test and Testable Design using HDL models and Architectures -Zainalabedin Navabi, Springer International Ed.,

REFERENCES:

1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing- Bushnell & Vishwani D.Agarwal,Springers.
3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

SYSTEM ON CHIP ARCHITECTURE (PE - III)

UNIT -I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT -II

Processors: Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT -III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multilevel Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction.

UNIT -IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT -V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JEPG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Eed., 2000, Addison Wesley Professional.

REFERENCES:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., Springer,2004.
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, Kluwer Academic Publishers,2001.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

EMBEDDED SOFTWARE ENGINEERING (PE – III)

UNIT -I

Software Engineering of Embedded and Real-Time Systems: Software engineering, Embedded systems, Embedded systems are reactive systems, Real-time systems, Soft and Hard Real-Time systems, Efficient execution and the execution environment, Resource management, Challenges in real-time system design.

UNIT -II

The embedded system software build process, Distributed and multi-processor architectures, Software for embedded systems, Super loop architecture, Power-save super loop, Window lift embedded design, Hardware abstraction layers (HAL) for embedded systems, HW/SW prototyping, Industry design chain, Different types of virtual prototypes, Architecture virtual prototypes, Software virtual prototypes.

UNIT -III

Events, Triggers and Hardware Interface to Embedded Software: Events and triggers, Event system, Event handle, Event methods, Event data structure, Reentrancy, Disable and enable interrupts, Semaphores, Implementation with Enter/ExitCritical, Event processing, Integration, Triggers, Blinking LED, Design idea, Tick timer, Trigger interface, Trigger descriptor, Data allocation, SetTrigger, IncTicks, Making it reentrant, Initialization, Real-time aspects, Introduction to Hardware Interface, Collaboration, System integration, Launching tasks in hardware, Debug hooks, Compile-time switches, Build-time switches, Run-time switches, Self-adapting switches, Difficult hardware interactions, Testing and troubleshooting.

UNIT -IV

Embedded Software Programming and Operating Systems: Introduction, Principles of high-quality programming, Readability, Maintainability, Testability, Starting the embedded software project, Libraries from third parties, Team programming guidelines, Syntax standard, Conditional compilation, Foreground/background systems, Real-time kernels, RTOS (real-time operating system), Critical sections, Task management, Preemptive scheduling, Context switching, Interrupt management, Non-kernel-aware interrupt service routine (ISR), Processors with multiple interrupt priorities, The clock tick (or system tick), Wait lists, Time management, Resource management, Synchronization, Message passing, Flow control, Clients and servers, Memory management

UNIT -V

Software Reuse and Performance Engineering in Embedded Systems: Kinds of software reuse, Implementing reuse by layers,Arbitrary extensibility, Ebedded Software for Performance, The code optimization process, Using the development tools, Compiler optimization

TEXTBOOK:

1. Software Engineering for Embedded Systems: Methods, Practical Techniques, and Applications, by Oshana, Robert; Kraeling, Mark, “Newnes” Publishers, 2013.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

EMBEDDED REAL TIME OPERATING SYSTEMS (PE – III)

Prerequisite: Computer Organization and Operating System

Course Objectives: The objectives of this course are:

- To provide broad understanding of the requirements of Real Time Operating Systems.
- To make the student understand, applications of these Real Time features using case studies.

Course Outcomes

- Be able to explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
- Able describe how a real-time operating system kernel is implemented.
- Able explain how tasks are managed.
- Explain how the real-time operating system implements time management.
- Discuss how tasks can communicate using semaphores, mailboxes, and queues.
- Be able to implement a real-time system on an embedded processor.
- Be able to work with real time operating systems like RT Linux, Vx Works, MicroC /OS- II, Tiny OS

UNIT -I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT -II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.
.

UNIT -III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

Case Studies of RTOS:RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOK:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

REFERENCES:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal,TMH, 2007.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

HARDWARE AND SOFTWARE CO-DESIGN (PE – IV)

Course Outcomes:

- To acquire the knowledge on various models of Co-design.
- To explore the interrelationship between Hardware and software in a embedded system
- To acquire the knowledge of firmware development process and tools during Co-design.
- Understand validation methods and adaptability.

UNIT - I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

REFERENCES:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami,Kluwer Academic Publishers, 2002.
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

LOW POWER VLSI (PE – IV)

Pre-Requisite: VLSI

Course Objectives: The objectives of this course are to:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design adders, Multipliers and memory circuits with low power dissipation.

Course Outcomes:

- The student will get to know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

UNIT - I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling **–** VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT- III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT - IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCES:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

AD-HOC AND WIRELESS SENSOR NETWORKS (PE - IV)

Prerequisite: Wireless Sensor Networks

Course Objectives: The objectives of this course are to make the student

- To study the fundamentals of wireless Ad-Hoc Networks.
- To study the operation and performance of various Adhoc wireless network protocols.
- To study the architecture and protocols of Wireless sensor networks.

Course Outcomes: On completion of this course student will be able to

- Students will be able to understand the basis of Ad-hoc wireless networks.
- Students will be able to understand design, operation and the performance of MAC layer protocols of Adhoc wireless networks.
- Students will be able to understand design, operation and the performance of routing protocol of Adhoc wireless network.
- Students will be able to understand design, operation and the performance of transport layer protocol of Adhoc wireless networks.
- Students will be able to understand sensor network Architecture and will be able to distinguish between protocols used in Adhoc wireless network and wireless sensor networks.

UNIT - I

Wireless LANs and PANs: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.
AD HOC WIRELESS NETWORKS: Introduction, Issues in Ad Hoc Wireless Networks.

UNIT - II

MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT - III

Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT – IV

Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

REFERENCES:

1. Ad-Hoc Mobile Wireless Networks: Protocols & Systems, C. K. Toh , 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

EMBEDDED SYSTEMS LAB (LAB – III)

List of Experiments:

1. **Functional Testing Of Devices**
   Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems**
   Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming**
   Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430**
   Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity**
   Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator**
   Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V).
7. **Dice Game Simulation**
   Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface**
   Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device**
   Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board**
    Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server(eg: Apache) and thereby host the website.
11. **Webcam Server**
    Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission**
    Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz).

Note : Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

SIMULATION LAB (LAB – IV)

List of Experiments:

1. Overview of EDA Tools Micro Wind / Cadence / Electric
2. Dynamic Charecteristics of CMOS Inverter
3. Design and Simulation of Combinational Circuits
4. Design and Simulation of Sequential Circuits
5. Design and Simulation of Source Follower Circuits
6. Design and Simulation of Cascode Amplifier
7. Design and Simulation of Current Mirror Amplifier
8. Design and Simulation of Differential Amplifier

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- II YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
EMBEDDED NETWORKS (PE – V)

Prerequisite: Computer Networks.

Course Objectives:

- To elaborate on the conceptual frame work of physical layer and topological issues of networking in Embedded Systems.
- To emphasis on issues related to guided and unguided media with specific reference to Embedded device level connectivity.

Course Outcomes:

- Expected to acquire knowledge on communication protocols of connecting Embedded Systems.
- Expected to master the design level parameters of USB and CAN bus protocols.
- Understand the design issues of Ethernet in Embedded networks.
- Acquire the knowledge of wireless protocols in Embedded domain.

UNIT -I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface(SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT -II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT -III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables,Connections and network speed – Design choices: Selecting components –Ethernet Controllers –
Using the internet in local and internet communications – Inside the Internet protocol.

UNIT -IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.

2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCES:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- II YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

SOFT COMPUTING TECHNIQUES (PE - V)

UNIT - I

Fundamentals of Neural Networks & Feed Forward Networks: Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT - II

Associative Memories & ART Neural Networks: Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT - III

Fuzzy Logic & Systems: Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT - IV

Genetic Algorithms: Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT - V

Hybrid Systems: Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications - S. Rajasekaran, G. A. Vijayalakshmi Pai, PHI, New Delhi, July 2011.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

REFERENCES

1. Artificial Neural Networks - Dr. B. Yagananarayana, PHI, New Delhi, , 1999.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- II YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS

VLSI SIGNAL PROCESSING (PE - V)

Course Outcomes: On successful completion of the module, students will be able to:

- Ability to modify the existing or new DSP architectures suitable for VLSI.
- Understand the concepts of folding and unfolding algorithms and applications.
- Ability to implement fast convolution algorithms.
- Low power design aspects of processors for signal processing and wireless applications.

UNIT -I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems

Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V

Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, Wiley Inter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall, 1985.

REFERENCES:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing – Medisetti V. K, IEEE Press (NY), 1995.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

ENGLISH FOR RESEARCH PAPER WRITING (Audit Course - I & II)

Prerequisite: None

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT-I:
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

DISASTER MANAGEMENT (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countries they work in

UNIT-I:
Introduction:
Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.
Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:
Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:
Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:
Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:
Disaster Mitigation:
Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, “Disaster Management in India: Perspectives, issues and strategies “’New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.),” Disaster Mitigation Experiences and Reflections”, Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies”, Deep &Deep Publication Pvt. Ltd., New Delhi.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

SANSKRIT FOR TECHNICAL KNOWLEDGE (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes: Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

UNIT-I:
Alphabets in Sanskrit,

UNIT-II:
Past/Present/Future Tense, Simple Sentences

UNIT-III:
Order, Introduction of roots,

UNIT-IV:
Technical information about Sanskrit Literature

UNIT-V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/ REFERENCES:

1. “Abhyaspustakam” – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. “India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

VALUE EDUCATION (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

UNIT-I:
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:
Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

CONSTITUTION OF INDIA (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working), **Philosophy of the Indian Constitution:** Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

PEDAGOGY STUDIES (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT-I:
Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:
Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:
Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:
Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

STRESS MANAGEMENT BY YOGA (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To achieve overall health of body and mind
- To overcome stress

Course Outcomes: Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT-I:
Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:
Yam and Niyam.

UNIT-III:
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:
Asan and Pranayam

UNIT-V:
i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (DSCE)

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes: Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.