JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH. IN EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS
EFFECTIVE FROM ACADEMIC YEAR 2019-20 ADMITTED BATCH

R19 COURSE STRUCTURE AND SYLLABUS

I YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - I	RTL Simulation and Synthesis with PLDs	3	0	0	3
Professional Core - II	Microcontrollers & Programmable Digital Signal Processors	3	0	0	3
Professional Elective - I	1. Digital Signal & Image Processing 2. Programming Languages for Embedded Software 3. Memory Technologies	3	0	0	3
Professional Elective - II	1. Parallel Processing 2. Advanced Computer Architecture 3. CAD of Digital Systems	3	0	0	3
Lab - I	RTL Simulation and Synthesis with PLDs Lab	0	0	3	2
Lab - II	Microcontrollers & Programmable Digital Signal Processors Lab	0	0	3	2
	Research Methodology & IPR	2	0	0	2
Audit - I	Audit Course - I	2	0	0	0
	Total	**16**	**0**	**6**	**18**

I YEAR II – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - III	Analog and Digital CMOS VLSI Design	3	0	0	3
Professional Core - IV	System Design with Embedded Linux	3	0	0	3
Professional Elective - III	1. Advanced Digital Signal Processing 2. SOC Design 3. Low Power VLSI Design	3	0	0	3
Professional Elective - IV	1. Communications Buses & Interfaces 2. Network Security & Cryptography 3. Physical Design Automation	3	0	0	3
Lab - III	Analog and Digital CMOS VLSI Design Lab	0	0	3	2
Lab - IV	System Design with Embedded Linux Lab	0	0	3	2
	Mini project with Seminar	0	0	4	2
Audit - II	Audit Course- II	2	0	0	0
	Total	**14**	**0**	**10**	**18**

III – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Elective - V	1. IOT and its Applications 2. AI and Machine Learning 3. Nano Materials and Nano Technology	3	0	0	3
Open Elective	Open Elective	3	0	0	3
Dissertation	Dissertation Work Review - II	0	0	12	6
	Total	**6**	**0**	**12**	**12**

II YEAR II - SEMESTER

Course Code	Course Title	L	T	P	Credits
Dissertation	Dissertation Work Review - III	0	0	12	6
Dissertation	Dissertation Viva-Voce	0	0	28	14
	Total	**0**	**0**	**40**	**20**

***For Dissertation Work Review - I, Please refer 7.8 in R19 Academic Regulations.**

Audit Course I & II:

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by yoga
8. Personality Development Through Life Enlightenment Skills

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH. I YEAR - I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

RTL SIMULATION AND SYNTHESIS WITH PLDs (PC – I)

Course Outcomes: At the end of the course, students will demonstrate the ability to:

1. Familiarity of Finite State Machines, RTL design using reconfigurable logic.
2. Design and develop IP cores and Prototypes with performance guarantees
3. Use EDA tools like Cadence, Mentor Graphics and Xilinx

UNIT-I

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

UNIT-II

Design entry by Verilog/VHDL/FSM, Verilog AMS.

UNIT-III

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

UNIT-IV

Design for performance, Low power VLSI design techniques. Design for testability.

UNIT-V

IP and Prototyping: IP in various forms: RTL Source, Encrypted Source, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping

TEXTBOOKS:

1. Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
2. Donald D Givone, “Digital principles and Design”, TMH

REFERENCES:

1. Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
2. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
3. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx.
4. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books.

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M.TECH. I YEAR - I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS (PC – II)

Course Outcomes: At the end of this course, students will be able to;

1. Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
2. Identify and characterize architecture of Programmable DSP Processors
3. Develop small applications by utilizing the ARM processor core and DSP processor-based platform.

UNIT-I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT-II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT-III

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT-IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT-V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations

TEXTBOOKS:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications”, TMH, 2nd Edition

REFERENCES:

1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication.
2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
3. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

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M.TECH. I YEAR - I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

DIGITAL SIGNAL AND IMAGE PROCESSING (PE – I)

Course Outcomes: At the end of this course, students will be able to

1. Analyze discrete-time signals and systems in various domains
2. Design and implement filters using fixed point arithmetic targeted for embedded platforms
3. Compare algorithmic and computational complexities in processing and coding digital images.

UNIT-I
Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.

UNIT-II
Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation.

UNIT-III
Fixed point implementation of filters – challenges and techniques.

UNIT-IV
Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – JPEG and JPEG 2000.

UNIT-V
Color Image processing – Handling multiple planes, computational challenges.

TEXTBOOKS:

1. J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
2. Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition

REFERENCES:

1. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006
2. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
3. Keshab Parhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India

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M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE (PE – I)

Course Outcomes: At the end of this course, students will be able to

1. Write an embedded C application of moderate complexity.
2. Develop and analyze algorithms in C++.
3. Differentiate interpreted languages from compiled languages.

UNIT-I

Embedded 'C' Programming

- Bitwise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT -II

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT-III

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions

UNIT-IV

Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling: try-catch-throw, Multiple Exceptions.

UNIT-V

Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables,
Inter process Communication Threads, Compilation & Line Interfacing.

TEXTBOOKS:

1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011

REFERENCES:

1. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005

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M.TECH. I YEAR - I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

MEMORY TECHNOLOGIES (PE – I)

Course Outcomes: At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Know, how of the state-of-the-art memory chip design

UNIT-I

Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT-II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT-III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT-IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-Access Memories (MRAMs), Experimental Memory Devices.

UNIT-V

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXTBOOKS:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition

REFERENCE:

1. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability, PHI

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EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

PARALLEL PROCESSING (PE – II)

Course Outcomes: At the end of this course, students will be able to

1. Identify limitations of different architectures of computer
2. Analysis quantitatively the performance parameters for different architectures
3. Investigate issues related to compilers and instruction set based on type of architectures.

UNIT-I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability, Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT-II

VLIW processors

Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT-III

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT-IV

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

UNIT-V

Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

TEXTBOOKS:

1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition
2. Kai Hwang, “Advanced Computer Architecture”, TMH

REFERENCES:

1. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.
2. William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition
3. Kai Hwang, Zhiwei Xu, “Scalable Parallel Computing”, MGH
4. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.
5. System Design with Embedded Circuits (PE-2.2)

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ADVANCED COMPUTER ARCHITECTURE (PE – II)

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", Mc Graw Hill.
3. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

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M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

CAD FOR DIGITAL SYSTEMS (PE – II)

Course Outcomes: At the end of this course, students will be able to

1. Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
2. Study of various phases of CAD, including simulation, physical design, test and verification.
3. Demonstrate knowledge of computational algorithms and tools for CAD.

UNIT-I

Introduction to VLSI Methodologies –Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

UNIT-II

VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

UNIT-III

General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement, routing.

UNIT-IV

Simulation – logic synthesis, verification, high level Synthesis.

UNIT-V

MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

REFERENCES:

1. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”.
2. S.H. Gerez, “Algorithms for VLSI Design Automation”.

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M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

RTL SIMULATION AND SYNTHESIS WITH PLDs LAB (Lab – I)

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
2. Use EDA tools like Cadence, Mentor Graphics and Xilinx or equivalent tools

List of Experiments:

1. Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Enr/der, Priority enr, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3. Vending machines - Traffic Light controller, ATM, elevator control.
4. PCI Bus & arbiter and downloading on FPGA.
5. UART/ USART implementation in Verilog.
6. Realization of single port SRAM in Verilog.
7. Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

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EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB
(Lab – II)

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype s using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

12. To develop an assembly and C to compute Euclidian distance between any two points
13. To develop assembly and study the impact of parallel, serial and mixed execution
14. To develop assembly and C for implementation of convolution operation
15. To design and implement filters in C to enhance the features of given input sequence/signal

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M.TECH. I YEAR - I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

RESEARCH METHODOLOGY AND IPR

Prerequisite: None

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I:
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:
Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III:
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information

and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students’”
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”

REFERENCES:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

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M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

ANALOG AND DIGITAL CMOS VLSI DESIGN (PC – III)

Course Outcomes: At the end of this course, students will be able to

1. Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
2. Connect the individual gates to form the building blocks of a system.
3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

Digital CMOS Design:

UNIT-I:

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

UNIT-II

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.

Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT-III

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit.

Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design:

UNIT-IV

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT-V

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

TEXTBOOKS:

1. J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design perspective”, Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.

REFERENCES:

1. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
2. Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford, 3rd Edition.
3. R J Baker, “CMOS circuit Design, Layout and Simulation”, IEEE Inc., 2008.
4. Kang, S. and Leblebici, Y., “CMOS Digital Integrated Circuits, Analysis and Design”, TMH, 3rdEdition.
5. Pucknell, D.A. and Eshraghian, K., “Basic VLSI Design”, PHI, 3rd Edition

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M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

SYSTEM DESIGN WITH EMBEDDED LINUX (PC – IV)

Course Outcomes: At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Understand and create Linux BSP for a hardware platform

UNIT- I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling.
Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross tool chains

UNIT- II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT- III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules
Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules

UNIT- IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT- V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds, “Mastering Embedded Linux Programming” - Second Edition, PACKT Publications Limited.
2. Karim Yaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”, Auerbach Publications

REFERENCES:

1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014

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M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

ADVANCED DIGITAL SIGNAL PROCESSING (PE – III)

Course Outcomes: At the end of this course, students will be able to

1. To understand theory of different filters and algorithms
2. To understand theory of multirate DSP, solve numerical problems and write algorithms
3. To understand theory of prediction and solution of normal equations
4. To know applications of DSP at block level.

UNIT-I

Overview of DSP, Characterization in time and frequency, FFT Algorithms, Digital filter design and structures: Basic FIR/IIR filter design &structures, design techniques of linear phase FIR filters,IIR filters by impulse invariance, bilinear transformation, FIR/IIR Cascaded lattice structures, parallel realization of IIR.

UNIT-II

Multi rate DSP, Decimators and Interpolators, Sampling rate conversion, multistage decimator & interpolator, poly phase filters, QMF, digital filter banks, Applications in subband coding.

UNIT-III

Linear prediction & optimum linear filters, stationary random process, forward-backward linear prediction filters, solution of normal equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.

UNIT-IV

Adaptive Filters, Applications, Gradient Adaptive Lattice, Minimum mean square criterion, LMS algorithm, Recursive Least Square algorithm

UNIT-V

Estimation of Spectra from Finite-Duration Observations of Signals. Nonparametric Methods for Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation, Minimum-Variance Spectral Estimation, Eigen analysis Algorithms for Spectrum Estimation.

TEXTBOOKS:

1. J. G. Proakis and D.G. Manolakis, “Digital signal processing: Principles, Algorithm and Applications”, 4th Edition, Prentice Hall, 2007.
2. N. J. Fliege, “Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets”, 1st Edition, John Wiley and Sons Ltd, 1999.

REFERENCES:

1. Bruce W. Suter, “Multirate and Wavelet Signal Processing”,1st Edition, Academic Press, 1997.
2. M. H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley & Sons Inc., 2002.
3. S. Haykin, “Adaptive Filter Theory”, 4th Edition, Prentice Hall, 2001.
4. D. G. Manolakis, V. K. Ingle and S. M. Kogon, “Statistical and Adaptive Signal Processing”, McGraw Hill, 2000

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS
SOC DESIGN (PE – III)

Course Outcomes: At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches
2. Design SoC based system for engineering applications
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

UNIT-I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT-II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT-III

Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT-IV

Low power SoC design / Digital system, Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT-V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXTBOOKS:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006

REFERENCES:

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

LOW POWER VLSI DESIGN (PE – III)

Course Outcomes: At the end of the course, students will be able to:

1. Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
2. Characterize and model power consumption & understand the basic analysis methods.
3. Understand leakage sources and reduction techniques.

UNIT-I

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT-II

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.
Low Power Clock Distribution: Power dissipation in clock distribution, single driver

UNIT-III

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

UNIT-IV

Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

UNIT-V

Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

TEXTBOOKS

1. P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.

REFERENCES:

1. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
3. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

COMMUNICATION BUSES AND INTERFACES (PE – IV)

Course Outcomes: At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT-I

Serial Busses - Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I^2C, SPI

UNIT-II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT-III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT-IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT-V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

TEXTBOOKS:

1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems”, Lakeview Research, 2nd Edition
2. Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x
6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

NETWORK SECURITY AND CRYPTOGRAPHY (PE – IV)

Course Outcomes: At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT-I

Security: Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT-II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT-III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT-IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT-V

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition

REFERENCES:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

PHYSICAL DESIGN AUTOMATION (PE – IV)

Course Outcomes: At the end of the course, students will be able to:

1. Study automation process for VLSI System design.
2. Understanding of fundamentals for various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

UNIT -I

Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT -II

Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT -III

Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT -IV

Global routing: Problem formulation, classification of global routing, Maze routing algorithms, Line-Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.

Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi-Layer channel routing, Algorithms, Switch box routing.

UNIT -V

Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.

Via Minimization: Constraint and Unconstrained via minimization.

Clock and Power Routing: Clocking schemes, design considerations for the clock , Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS

1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

ANALOG AND DIGITAL CMOS VLSI DESIGN LAB (Lab – III)

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Design digital and analog Circuit using CMOS.
2. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

List of Experiments:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
   a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
   c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
   d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV
      To extract Vth use the following procedure.
      i. Plot gm vs VGS using NGSPICE and obtain peak gm point.
      ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.
      iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.

   Tabulate your result according to technologies and comment on it.

2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
   a) Perform the following
      i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)
   c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)

3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4) Perform the following

a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13um process.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.

ii. Calculate input bias voltage if bias current=50uA.

iii. Use Ngspice and obtain the bias current. Compare its value with 50uA.

iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW

vi. Use Ngspice to determine input voltage range of the amplifier

5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA.

Note: Adjust accuracy options of the simulator (setup->options in GUI).

Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.

ii. Draw the schematic of INA.

iii. Obtain parameters of the op-amp macro model such that

a. low-frequency voltage gain = 5x104,

b. unity gain BW (fu) = 500KHz,

c. input capacitance=0.2pF,

d. output resistance = ,

e. CMRR=120dB

iv. Draw schematic diagram of CMRR simulation setup.

v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.

6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.

a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.

b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.

c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.

d) Use interconnect length obtained and connect the second and third inverter.
Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

SYSTEM DESIGN WITH EMBEDDED LINUX LAB (Lab – IV)

List of Experiments

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- II YEAR- I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

IOT AND ITS APPLICATIONS (PE – V)

Course Outcomes: At the end of this course, students will be able to

1. Understand the concept of IOT and M2M
2. Study IOT architecture and applications in various fields
3. Study the security and privacy issues in IOT.

UNIT-I

IoT & Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.

UNIT-II

M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT-III

IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model-Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture-Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

UNIT-IV

IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

UNIT-V

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues,

TEXTBOOKS

1. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-on-Approach)”, 1st Edition, VPT, 2014.
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1st Edition, Apress Publications, 2013.
3. Cuno Pfister, “Getting Started with the Internet of Things”, O Reilly Media, 2011.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- II YEAR- I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

AI AND MACHINE LEARNING (PE – V)

UNIT- I

Supervised Learning (Regression/Classification)

Basic methods: Distance-based methods, Nearest-Neighbours, Decision Trees, Naive Bayes Linear models: Linear Regression, Logistic Regression, Generalized Linear Models Support Vector Machines, Nonlinearity and Kernel Methods

Beyond Binary Classification: Multi-class/Structured Outputs, Ranking

UNIT- II

Unsupervised Learning

Clustering: K-means/Kernel K-means

Dimensionality Reduction: PCA and kernel PCA

Matrix Factorization and Matrix Completion

Generative Models (mixture models and latent factor models)

UNIT- III

Evaluating Machine Learning algorithms and Model Selection, Introduction to Statistical Learning Theory, Ensemble Methods (Boosting, Bagging, Random Forests)

UNIT- IV

Biological foundations to intelligent Systems: Artificial Neural Networks.

Single layer and Multilayer Feed Forward NN, LMS and Back Propagation. Algorithm, Feedback networks and Radial Basis Function Networks

UNIT- V

Fuzzy Logic, Knowledge Representation and Inference Mechanism, Defuzzification Methods Fuzzy Neural Networks and some algorithms to learn the parameters of the network like GA

TEXTBOOKS:

1. Kevin Murphy, Machine Learning: A Probabilistic Perspective, MIT Press, 2012
2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning, Springer 2009 (freely available online)
3. Christopher Bishop, Pattern Recognition and Machine Learning, Springer, 2007.
4. J M Zurada , “An Introduction to ANN”,Jaico Publishing House
5. Simon Haykins, “Neural Networks”, Prentice Hall

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH.- II YEAR- I SEMESTER
EMBEDDED SYSTEMS & VLSI DESIGN/VLSI & EMBEDDED SYSTEMS

NANOMATERIALS AND NANOTECHNOLOGY (PE - V)

Course Outcomes: At the end of the course, students will be able to:

1. To understand the basic science behind the design and fabrication of nano scale systems.
2. To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
4. To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems

UNIT - I

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms – specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostrutures – precipitative – reactive –hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT - II

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nanomaterials, Three dimensional nanomaterials. Low-Dimensional Nanomaterials and its Applications, Synthesis, Properties, and Applications of Low-Dimensional Carbon-Related Nanomaterials.

UNIT - III

Micro- and Nanolithography Techniques, Emerging Applications Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT - IV

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT’s - Multi-walled nanotubes, Single-walled nanotubes Optical properties of CNT’s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNT's.

UNIT - V

Ferroelectric materials, coating, molecular electronics and nanoelectronics, biological and environmental, membrane based application, polymer based application.

TEXT BOOKS

1. Kenneth J. Klabunde and Ryan M. Richards, “Nanoscale Materials in Chemistry”, 2 edition, John Wiley and Sons, 2009.
2. I Gusev and A A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1 st Indian edition by Viva Books Pvt. Ltd. 2008.
3. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, “Nanoscience and

4. Nanotechnology", Tata McGraw Hill Education 2012.

REFERENCE BOOKS

1. Bharat Bhushan, "Springer Handbook of Nanotechnology", Springer, 3 rd edition, 2010.
2. Kamal K. Kar, "Carbon Nanotubes: Synthesis, Characterization and Applications", Research Publishing Services; 1 st edition, 2011, ISBN-13: 978-9810863975.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (ES & VLSI DESIGN/VLSI & ES)

ENGLISH FOR RESEARCH PAPER WRITING (Audit Course - I & II)

Prerequisite: None

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT-I:
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (ES & VLSI DESIGN/VLSI & ES)

DISASTER MANAGEMENT (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countries they work in

UNIT-I:
Introduction:
Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.
Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:
Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:
Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:
Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:
Disaster Mitigation:
Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, “Disaster Management in India: Perspectives, issues and strategies “’New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.),” Disaster Mitigation Experiences and Reflections”, Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies”, Deep &Deep Publication Pvt. Ltd., New Delhi.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (ES & VLSI DESIGN/VLSI & ES)

SANSKRIT FOR TECHNICAL KNOWLEDGE (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes: Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

UNIT-I:
Alphabets in Sanskrit,

UNIT-II:
Past/Present/Future Tense, Simple Sentences

UNIT-III:
Order, Introduction of roots,

UNIT-IV:
Technical information about Sanskrit Literature

UNIT-V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/ REFERENCES:

1. “Abhyaspustakam” – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. “India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (ES & VLSI DESIGN/VLSI & ES)

VALUE EDUCATION (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

UNIT-I:
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:
Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
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CONSTITUTION OF INDIA (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working), **Philosophy of the Indian Constitution:** Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (ES & VLSI DESIGN/VLSI & ES)

PEDAGOGY STUDIES (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT-I:
Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:
Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:
Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:
Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (ES & VLSI DESIGN/VLSI & ES)

STRESS MANAGEMENT BY YOGA (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To achieve overall health of body and mind
- To overcome stress

Course Outcomes: Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT-I:
Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:
Yam and Niyam.

UNIT-III:
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:
Asan and Pranayam

UNIT-V:
i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech. (ES & VLSI DESIGN/VLSI & ES)

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes: Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.