

ABOUT CoreEL TECHNOLOGIES

CoreEL Technologies, a Customer Application Specific Product & Solutions (CASPS) company offers INNOVATIVE solutions from its diverse portfolio of expertise that includes Intellectual Property (IP) cores, System Design, Manufacturing, Sustenance and OEM solutions in the form of EDA tools, CAE tools, COTS products and Technology Training.

CoreEL's strength lies in its ability to blend deep domain knowledge with the right ingredients across its portfolio of offerings. It is a leading developer of advanced electronic system level products and solutions to three primary markets – Aerospace & Defence, Digital Media Broadcast and Universities & Institutions of higher learning.

CoreEL Technologies won the 'Best Manufacturing Company (MSME)' and one of the 'Top 25 Innovative Company' awards at the CII Innovation Awards 2015. CoreEL Technologies is the recipient of India Today's #MakeInIndia Emerging Entrepreneur Award 2018. CoreEL was selected in the Electronics category for this award.

About CoreEL University Programme

CoreEL University Program provides Eco-System support to Indian Academia in Engineering Higher Education, in the field

of embedded systems thereby enabling the delivery of quality education. CoreEL University achieves this by providing state of the art products from XILINX, MENTOR GRAPHICS, STRATASYS, MATLAB, ANSYS, VxWorks (WIND RIVER), Speed-goat (Rapid Controller Prototyping, Hardware-in-the-Loop simulation, and deployment,) PCB Design Tools from Mentor

Graphics ,Analog Discovery Kits from Digilent (Analog Discovery kit can replace the conventional regulated power supply, Function Generator, Oscilloscope, and smaller parts like Bread board etc with one portable, compact and power effective and low cost solution!) to universities Multiyear application engineering support on these products Faculty and student training, providing industry specific inputs to update the curriculum and helping universities set up Centers of Excellence in Embedded Systems arena.

COORDINATORS

Dr. Ch. Venkata Ramana Reddy
Director, UIIC, JNTUH

Dr. M. Madhavi Latha
Professor in ECE & Coordinator-CVED
JNTUH CEH

RESOURCE PERSONS

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A WORKSHOP ON CUSTOM IC & PHYSICAL DESIGN USING MENTOR EDA TOOLS

From
19-08-2019 to 21-08-2019

(UNDER TEQIP-III)

Organized by
**University Industry Interaction Centre
(UIIC), JNTUH, HYDERABAD**



In Association with



ABOUT UNIVERSITY

Jawaharlal Nehru Technological University, the First Technological University of India, was established on 2nd October 1972 in Andhra Pradesh with head quarters located in Hyderabad.

The University is one of the premier Universities in India, accredited by NAAC with 'A' Grade. After successful and proven levels of appreciated existence and stature spanning over 36 years, JNTU has been divided into four different Universities by Govt. of Andhra Pradesh, through Act No.30, Dt. 24th September, 2008.

JNTU Hyderabad is one among the four Universities. Its Constituent college, "JNTUH College of Engineering, Hyderabad" is regarded as a pioneer in Technical Education and is a flagship College of the University. Other constituent colleges of JNTUH are located at Jagityal, Sultanpur, Manthani and other academic units at Hyderabad campus.

Directorate of University Industry Interaction Centre (D-UIIC)

JNTU Hyderabad has been a pioneer in promoting industry-academia interaction and the scope of the activities has been steadily growing. In this endeavour, JNTUH has established a Directorate of University Industry Interaction Centre (UIIC) in the year, 2009.

Industry interactions relating to Engineering and Technology, Basic and Applied Sciences, Pharmacy and Management come under the umbrella of University Industry Interaction Centre.

The main focus of UIIC is to bridge the gap between Industry requirements and Academic delivery.

The UIIC carries forward the interaction of University with the industrial bodies of Public, Private and Government sector Organizations.

Objectives of UIIC

- UIIC helps the Industry to hire the right talent from its students' community at the right time.
- UIIC facilitates the students' internships, academic projects, training programs and Placements for the Students by the Industries.
- Facilitates the training, research and Consultancy projects by the Industries to the faculty.
- Organizes several collaborative programs as seminars, workshops, industry visits etc for the Students and Faculty.

REGISTRATION DETAILS

There is no Registration Fee

For Free Registration follow the link:

<https://forms.gle/uNTzYrHZB3UJssTn6>

Lunch, Tea and Snacks will be provided for the Participants at the Venue

Limited seats: Registration is on first come first serve basis. Selected participants will be informed by Email on 16th Aug, 2019.

Last date for registration: 15th Aug, 2019.

Travel/Accommodation

Participants are required to make their own arrangements for travel, local conveyance and accommodation.

Address for Correspondence

Dr. M. Madhavi Latha

Professor & Coordinator - CVED Department of ECE, JNTUH
CEH Cell: 9848506611, Email: mlmakkena@yahoo.com

Venue: UIIC, JNTUH (Admissions Block)

Time: 10:00 AM to 5:00 PM

Who should attend?

- Faculty from Universities and Colleges

TRAINING AGENDA:

Day 1 : 19-08-2019

- Basics of ASIC Design and ASIC Vs FPGAs
- Full Custom Flow and Semi Custom Design Flow
- Latest Advancements VLSI Industry
- Full Custom Design Flow (Digital/Amplifiers Circuits)
- Schematic Entry, Spice Models, Simulation (Amplifiers and Digital Circuits)
- DC, AC, Power and Transient Analysis
- Hands-on Session

Day 2 : 20-08-2019

- Layout entry (Amplifiers & Digital Circuits)
- Placement & Routing
- Physical Verification Using Industry Standard Calibre Tool
- DRC, LVS and PEX
- Back Annotation/Post Layout Simulation
- Hands-on session

Day 3 : 21-08-2019

- Semi Custom Design Flow (Physical Design Flow)
Verilog Entry: Simulation and Synthesis
Schematic/Layout Design from Verilog Netlist
- Physical Design Flow (RTL to GDSII)
- Floor Planning, Placement
- Routing and Physical Verification
- Generating GDSII file and Analysis

Key Learning Outcome's

- Knowledge on VLSI Design and Manufacturing process
- Able to use Design Kit for Design and Verification
- Complete idea on VLSI Design Methodologies
- Ability to do Research/Academic Projects
- Hands-on Practice over Industry Standard EDA Tools