Jawaharlal Nehru Technological University, the **First Technological University** of India, was established on 2nd October 1972 in Andhra Pradesh with head quarterslocated in a historical city **Hyderabad.** The University is one of the premier Universities in India accredited by **NAAC**with **'A'** Grade. After successful and proven levels of appreciated existence and stature spanning over 36 years, JNTU has been divided into four different universities by Govt. of Andhra Pradesh, through Act No.30, Dt. 24th September, 2008. One of the constituent colleges of the University **"JNTUH College of Engineering, Hyderabad"** is regarded as a pioneer in shaping the excellence of some of the leading organizations of the industry, by churning out the finest professionals with a resolve to scale greater heights in the technological scenario, every year. Other constituent college of JNTUH is located at Jagityal and 11 other academic units at Hyderabad campus.

The Department of **Electronics & Communication Engineering** established in 1973, is instrumental in molding the careers of students and helping them to become world-class professionals. The department is offering UG, PG, Research and Collaborative Programmes with well experienced faculty and as well as established laboratories. Besides highly qualified and experienced staff and well-equipped laboratories, the Department has been awarded ***8.1*** points out of ***10*** by the **State Board of Technical Education.**

Entuple Technologies Pvt., Ltd.:

Entuple is a next generation solutions enabler in cutting edge technologies. Head Quartered at Bangalore, India, Entuple delivers world class products & solutions in Applied Electromagnetics, Semiconductor and System Design & Reliability, Drivers & Power Systems, Telecom, Mechanical and Civil sector. We do offer R & D consulting across technologies. Our niche services include – IC fabrication alliance, Post silicon validation and more. We cater to wide range of customers in semiconductor, manufacturing, defense & aerospace and academia.

About the FDP/ Short Term Course:

VLSI technology has gone through rapid strides in last few decades. Despite digital processing of signals, advent of digital architecture and rapid growth of IC design technology, the basic abstraction layer for complex chipsets continuous to be Analog components. Analog circuit & layout design continuous to get more and more complex due to ever increasing demand for power, area and cost effective solutions in digital and analog IC design. Industry efforts are focused towards optimizing designs for better performance, area & energy and other key factors. Industry is looking at competent manpower to address these challenges on an ongoing basis. Academia is the main source of manpower to industry. Quality manpower from campuses is one of the key expectations of industry. Entuple believes in a philosophy of empowering faculty champions to groom competent future engineers of industry. The various learning activities driven by Entuple are focused towards this objective.

This Faculty Development Program (FDP) or Short Term Course (STC) program is designed to provide deeper aspects of Analog Circuit Design layout concepts. The program provides the industry ways of working environment for participants. It progressively builds the concepts with a kick start on functional blocks such as current mirrors, repeaters, operational amplifiers and delivers deep insights on characterization.

The program also caters to the needs of research scholars pursuing their research in custom IC Design/ Analog circuit and Layout. This program also benefits practicing engineers to fine tune their skill and work on analog circuit and layout design more effectively in their deliverables.

Key Learning Outcomes:

At the end of the program you will be able to:

- Analyze the performance specification requirements and identify the suitable circuit topologies
- Characterize the PDK for device analog model parameters
- Synthesize basic and OP-AMP amplifier circuit topologies
- Design CMOS Amplifier circuits for given DC and AC performance parameters
- Develop programmed spread sheets for amplifier design automation
- Design and characterize a seven – pack CMOS Compensated OP-AMP at the schematic design entry level
- Derive layout constraints for the physical design of the OP-AMP and carry out DRC and LVS
- Carry out the physical verification and parasitic extraction.
- Back Annotate and carry out Post Layout Simulation/ Characterization

Who should attend?

- Practicing engineers in Analog circuit and layout design
- Faculty involved in teaching Analog CMOS IC Design and Analog Mixed Signal design courses
- Research scholars pursuing research in Analog circuit and Layout, devicecharacterization and more.
- UG/PG students aspiring to get started with concepts of Analog circuit and layout foundation and planning for a career in semiconductor industry.

Course Outline and Structure

Day 1: Fundamentals of Analog Signal Processing – CMOS Amplifier Topologies and Performance

- Review of the generic amplifier performance parameters – Gain, Power Dissipation, Frequency Response, (Noise – optional, time permitting)
- Synthesis of Basic Amplifier Circuit Topologies
- Large and Small Signal DC Performance Analysis and Design of Basic Amplifiers
- Single and Differential Ended Signaling – Concept Illustration - What really is a *commonmode* signal?
- The Basic Ideal OP-AMP and its properties
- Lab1: PDK Device Characterization for Analog Model Parameters
- Lab 2: Hands – on Tutorial on Design and Simulation of a CS Amplifier for Large and Small Signal DC performance
- Lab 3: Design and Simulation of the Bias Circuit for the CS amplifier: Hands – on Tutorial

Day 2: Small Signal DC Design and Simulation of the Basic Differential Pair/ Analog Layout Design Concepts

- Interpreting the Design Specifications
- Design Methodology and Flow - Large Signal and Small Signal DC Design
- Analog Layout Design Concepts – Importance of Device Matching in Layouts; LDEs
- Lab 4: Design and Performance Characterization of CMOS Current Mirror (Schematic Design and Simulation)
- Lab 5: Layout Design of a CMOS Current Mirror
- Lab 6: DC Performance Characterization of the Basic CMOS Differential Amplifier (5 – Pack OP-AMP)

Day 3 – 4: Frequency Response and Compensation of Amplifiers – Performance Analysis

- Effect of the Amplifier BW limitations on Analog Signal Processing – Illustration
- Review of Transfer Functions and Frequency Response Plots; FB concepts and Effect of FB on Frequency Response, Stability and Compensation
- Gain – BW Enhancement Techniques – The CASCODE Stage
- Small Signal AC Performance of CS and Differential Pair
  - Lab 7: Design and Characterization of the CS amplifier for Small Signal DC and AC Performance
- Lab 8: Design and Characterization of Differential Pair for Small Signal DC and AC Performance

Day 5: Design and Performance Characterization of a 7 – Pack OPAMP

A Hands-on Tutorial for Schematic and Layout Design of a CMOS OP-AMP for the given Specifications and Characterization

Registration Fee:

- Faculty/Research Scholars: **Rs. 10,000/-**
- PG/UG students: **Rs.7,500/-**

Note: 1. DD/cash in favour of The Coordinator, AICD, JNTUH CEH, Hyderabad payable at Hyderabad.
2. Participants are advised to bring their personnel Laptops, if any. Future R&D guidance will be provided.

Limited seats: Registration is on first come first serve basis. Selected participants will be informed by mail by **1st July, 2017.** Seats will be blocked based on receipt of payment in advance.

Last date for registration: 30th June, 2017.

Travel/Accommodation

Participants are required to make their own arrangements for travel, local conveyance and accommodation.

Address for Correspondence

Dr. M. Madhavi Latha
Professor & Coordinator - CVED
Department of ECE, JNTUH CEH
Cell: 9848506611, Email: mlmakkena@yahoo.com

Venue: CVED, 2nd Floor, ECE Department, JNTUH CEH, **Time:**10:00 AM to 5:00 PM
Registration form: Down Load from **jntuhceh.ac.in or jntuh.ac.in** website.

A Faculty Development Program/Short Term Course on

"Analog IC Design (AICD) - Circuit and Layout Design Methodologiesusing Cadence Design Flow"

03rd-07th July, 2017

In collaboration with

ENTUPLE TECHNOLOGIES

Bangalore

Coordinator

Dr. M. Madhavi Latha

Professor in ECE &Coordinator-Center for Excellence in VLSI & Embedded Systems Design

Department of Electronics & Communication Engineering
JNTUH College of Engineering
Hyderabad-500 085, Telangana.

A Short Term Course on

"Analog IC Design- Circuit and Layout Design Methodologies Using Cadence Tools"

3-7 July, 2017

Registration Form

Name of the Applicant:……..……..

Designation:……

Gender: (M/F): …..

Educational Qualifications:…….

Address for Correspondence :(Including E-mail, Fax, Cell / Landline)

…….

Name of the Sponsoring Institute/Organization:……..

DD No:

Signature of the Applicant with date