ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

M.Tech.
Embedded Systems

(Effective for the students admitted from the Academic Year 2007-08)

Jawaharlal Nehru Technological University
Hyderabad – 500 085

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

M.Tech. (Embedded System) **w.e.f. 2005-06**

COURSE STRUCTURE AND SYLLABUS

Course No.	Subject	Contact Hrs. / wk.
FIRST SEMESTER		
	Micro Controllers for Embedded System Design	4
	Analog and Digital IC Design	4
	Embedded Systems Concepts	4
	System Modeling & Simulation	4
Elective –I		4
	VLSI Technology and Design	
	Advanced Computer Architecture	
	RF and Microwave Integrated Circuits	
Elective-II		4
	Digital Data Communications	
	Algorithm Analysis and Design	
	Image and Video Processing	
	HDL Simulation Laboratory	3
SECOND SEMESTER		
	Real Time Operating Systems for Embedded systems	4
	DSP Processors & Architectures	4
	CPLD and FPGA Architecture and Applications	4
	Embedded Software Design	4
Elective-III		4
	Scripting Language for VLSI Design Automation	
	Low Power VLSI Design	
	Advanced Digital filtering	
Elective-IV		4
	Design for Testability	
	Micro Electromechanical Systems	
	Wireless Communications and Networks	
	FPGA Synthesis Laboratory	3
THIRD & FOURTH SEMESTERS		
	SEMINAR	
	PROJECT	

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M.Tech. (Embedded System) **w.e.f. 2005-06**

I - Semester

MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT I

INTRODUCTION TO EMBEDDED SYSTEMS

Review of Micro controllers and their Features. 8 & 16 Bit Micro Controller Families (of Intel 8051) Flash Series, Motorola 68HC11; Micro Chip PIC 16C6X and Micro controller hardware. Embedded RISC Processor Architectures – ARM6TDMI(Advanced RISC Machines).

UNIT II

MICRO CONTROLLER INTERFACING

8051, 68HC11, PIC-16C6X and ATMEL External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT III

PROGRAMMING

Instruction sets and assembly language programme concepts and programming the 8051, 68HC11, PIC-16C6X Micro controller ARM6TDMI Core (SOC) and PIC-IDE.

UNIT IV

Interrupt synchronization – Interrupt vectors & priority, external interrupt design. Serial I/O Devices – RS232 Specifications, RS422/Apple Talk/ RS 423/RS435 & other communication protocols. Serial communication controller.

UNIT V

Ethernet Protocol, SDMA, Channels and IDMA Simulation, CPM Interrupt controller and CPM Timers, Power controls, External BUS Interface system Development and Debugging.

CASE STUDIES: Design of Embedded Systems using the micro controller – 8051/ARM6TDMI, for applications in the area of Communications, Automotives, industrial control.

SUGGESTED BOOKS

1. M.A. Mazadi & J.G. Mazidi, "The 8051 Micro Controller & Embedded Systems", Pearson Education. Asia (2000).
2. John B. Peatman, Designing with PIC Micro Controllers, Pearson Education.
3. Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole Thomas learning, 1999.
4. Cathey May and Silha
5. (Ed)., "The Power PC Architecture", Morgan Kauffman Press (1998).

I - Semester

ANALOG AND DIGITAL IC DESIGN

UNIT I

OPERATIONAL AMPLIFIERS: General considerations one – state op-amps, two stage op-amps – gains boosting stage – comparison – I/P range limitations slew rate. CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: simple CMOS, BJT current mirror, Cascode Wilson Wilder current mirrors. Common Source amplifier source follower, common gate amplifier

NOISE: Types of Noise – Thermal Noise – flicker noise – Noise in opamps – Noise in common source stage – noise band width.

UNIT II

PHASED LOCKED LOOP DESIGN: PLL concepts – The phase locked loop in the locked condition – Integrated circuit PLLs – phase Detector – voltage controlled oscillator – case study: Analysis of the 560 B Monolithic PLL.

SWITCHED CAPACITORS CIRCUITS: Basic Building blocks op-amps capacitors – switches – non-over lapping clocks – Basic operations and analysis – resistor equivalence of a switched capacitor – parasitic sensitive integrator – parasitic insensitive integrators – signal flow graph analysis – First order filters – switch sharing fully differential filters – charged injections – switched capacitor – gain circuits – parallel resistor – capacitor circuit – presettable gain cuicuit – other switched capacitor circuits – full wave rectifier – peak detector – sinusoidal oscillator .

UNIT III

LOGIC FAMILIES & CHARACTURISTICS: CMOS, TTL, ECL, logic families – CMOS / TTL, interfacing, comparison of logic families.

COMBINATIONAL LOGIC DESIGN USING VHDL: VHDL modeling for decoders, encoders, multipluxers, comparators, adders and subtractors.

SEQUENCIAL IC DESIGN USING VHDL: VHDL modeling for latches, flip flaps, counters, shift registers, FSMs.

UNIT IV

DIGITAL INTEGRADED SYSTEM BUILDING BLOCKS: Multiplexers and decoders – Barrel shifters – counters digital single bit adder

MEMORIES: ROM: Internal structure 2D decoding commercial types timing and applications

CPLD: XC 9500 series family CPLD architecture, functional block internal architecture. I/O block – internal structure.

FPGA: Conceptual of view of FPGA – classification based on CLB arrangement – programming technologies – XC 4000 series family architecture - CLB internal architecture – I/O block architecture.

UNIT V

COMPORATORS: Using an op-amp for a comparator – charge injection errors – latched comparator

NYQUIST RATE D/A CONVERTERS: Decoder based converter resistor storing converters folded resister string converter – Binary scale converters – Binary weighted resistor converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters..

NYQUIST RATE A/D CONVERTERS: Integrating coverters – successive approximation converters – DAC based successive approximation – flash converters time interleaved A/D converters.

REFERENCES

1. Analog Integrated Circuit Design by David A.Johns, Ken Martin, John Wiley & Sons.
2. Analysis and Design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley & Sons.
3. Design of Analog CMOS Integrated Circuits, Behzad Razavi. TMH
4. Digital Integrated Circuit Design by Ken Martin, Oxford University 2000
5. Digital Design Principles & Practices" by John F Wakerly, Pearson Education & Xilinx Design Series, 3rd Ed.(2002)

SUGGESTING READING

1. Ken Martin, Digital Integrated Circuit Design Oxford University, 2000.
2. John F Wakerly, "Digital Design Principles & Practices", Pearson Education & Xilinx Design Series, 3rd Ed.(2002).
3. Samir Palnitkar, "Verilog HDL-A Guide to Digital Design and Synthesis", Prentice Hall India, (2000).
4. Douglas J Smith, "HDL Chip Design, a Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs using VHDL or Verilog, Doone Publications, (1999).

I-Semester

EMBEDDED SYSTEMS CONCEPTS

UNIT I: AN INTRODUCTION TO EMBEDDED SYSTEMS

An Embedded system, processor in the system, other hardware units, software embedded into a system, exemplary embedded systems, embedded system – on – chip (SOC) and in VLSI circuit. Processor and memory organization – Structural Units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded systems, allocation of memory to program cache and memory management links, segments and blocks and memory map of a system, DMA, interfacing processors, memories and Input Output Devices.

UNIT II: DEVICES AND BUSES FOR DEVICE NETWORKS

I/O devices, timer and counting devices, serial communication using the "I2 C" CAN, profibus foundation field bus. and advanced I/O buses between the network multiple devices, host systems or computer parallel communication between the networked I/O multiple devices using the ISA, PCI, PCI-X and advanced buses.

UNIT III: DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM

Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism

UNIT IV: PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++, VC++ AND JAVA

Interprocess communication and synchronization of processes, task and threads, multiple processes in an application, problem of sharing data by multiple tasks and routines, interprocess communication.

UNIT V: HARDWARE – software co-design in an embedded system, embedded system project management, embedded system design and co-design issues in system development process, design cycle in the development phase for an embedded system, use of target systems, use of software tools for development of an embedded system, use of scopes and logic analysis for system, hardware tests. Issues in embedded system design.

TEXTBOOK

1. Embedded systems: Architecture, programming and design by Rajkamal, TMH

REFERENCEs

1. Embedded system design by Arnold S Burger, CMP
2. An embedded software primer by David Simon, PEA
3. Embedded systems design:Real world design be Steve Heath; Butterworth Heinenann, Newton mass USA 2002
4. Data communication by Hayt.

I - Semester

SYSTEM MODELING & SIMULATION

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

UNIT V

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

UNIT VI

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

UNIT VII

EVENT DRIVEN MODELS: Simulation diagrams, Queing theory, simulating queing systems, Types of Queues, Multiple servers.

UNIT VIII

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodogy.

TEXTBOOKS

1. System Modeling & Simulation, An Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modelling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCE BOOKS

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

I - Semester

VLSI TECHNOLOGY & DESIGN

(Elective – I)

UNIT – I:
REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi CMOS) Technology trends and projections.

UNIT – II:
BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds relationships, Threshold voltage V_t, G_m, G_{ds} and W_o, Pass Transistor, MOS,CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model,Latch-up in CMOS circuits.

UNIT – III:
LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias , Scalable Design rules ,Layout Design tools.

UNIT – IV:
LOGIC GATES & LAYOUTS: Static complementary gates, switch logic, Alternative gate circuits , low power gates, Resistive and Inductive interconnect delays.

UNIT – V:
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks Gate and Network testing.

UNIT – VI:
SEQUENTIAL SYSTEMS: Memory cells and Arrays, clocking disciplines, Design ,power optimization, Design validation and testing.

UNIT – VII:
FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power SOCs and Embedded CPUs, Architecture testing.

UNIT – VIII:
INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and printing; Hardware/Software Co-design, chip design methodologies- A simple Design example-

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf ,Pearson Education, fifth Indian Reprint,2005.

REFERENCES:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
   CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

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I - Semester

ADVANCED COMPUTER ARCHITECTURE
(Elective – I)

UNIT I

Fundamentals of Computer design- Technology trends- cost- measuring and reporting performance quantitative principles of computer design.

UNIT II

Instruction set principles and examples- classifying instruction set- memory addressing- type and size of operands- addressing modes for signal processing-operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler

UNIT III

Instruction level parallelism (ILP)- over coming data hazards- reducing branch costs –high performance instruction delivery- hardware based speculation- limitation of ILP

UNIT IV

ILP software approach- compiler techniques- static branch protection- VLIW approach- H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT V

Memory hierarchy design- cache performance- reducing cache misses penalty and miss rate – virtual memory- protection and examples of VM.

UNIT VI

Multiprocessors and thread level parallelism- symmetric shared memory architectures- distributed shared memory- Synchronization- multi threading.

UNIT VII

Storage systems- Types – Buses - RAID- errors and failures- bench marking a storage device- designing a I/O system.

UNIT VIII

Inter connection networks and clusters- interconnection network media – practical issues in interconnecting networks- examples – clusters- designing a cluster

TEXT BOOKS

1. Computer Architecture A quantitative approach 3rd edition John L. Hennessy & David A. Patterson Morgan Kufmann (An Imprint of Elsevier)

REFERENCES

1. "Computer Architecture and parallel Processing" Kai Hwang and A.Briggs International Edition McGraw-Hill.
2. Advanced Computer Architectures, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson.

I - Semester

R.F. MICROWAVE INTEGRATED CIRCUITS
(ELECTIVE- I)

UNIT I

Analysis and design of RF and microwave lines – Review of transmission lines, parallel plate transmission line, low frequency solution, high frequency solution, strip line and micro strip transmission lines, low frequency solution, high frequency properties of microslot line, co planer wave guides, coupled microstrip lines, spiral inductors – capacitors.

UNIT II

Microstrip/Stripline based filters. Resonators, phase shifters, micro strip based gyrators, circulators and isolators, directional couplers.

UNIT III

Microwave active devices – microwave transistors, GaAs FETS (Structures, equivalent circuit), Low noise amplifiers, power amplifiers, oscillators, detectors, mixers, modulators and switches.

UNIT IV

Technology of MICS: Deposition techniques – vacuum evaporation – Vacuum sputtering ion plating, MBE (Molecular Beam Epitaxy) – photo lithography, mask preparation, thick film technology, GaAs technology.

UNIT V

MIC Packaging: Component attachment bonding techniques, solder reflow techniques, input/output terminations, testing.

SUGGESTED BOOKS:

1. I. Kneppo and J. Fabian, "Microwave Integrated Circuit", London: Chapman & Hall, (1994).
2. M.W. Medley, "Microwave and RF circuit: Analysis, Synthesis and Design", Artech House, (1993).
3. R. Goyal, "Monolithic Microwave Integrated Circuits: Technology & Design", Artech House, (1989).
4. Y. Konishi, "Microwave Integrated Circuit", Dekker, New York: Marcel Dekker, (1991).

I - Semester

DIGITAL DATA COMMUNICATIONS
(ELECTIVE- II)

UNIT I
DIGITAL MODULATION TECHNIQUES
FSK , MSK , BPSK , QPSK , 8-PSK , 16-PSK , 8- QAM , 16- QAM , Band width efficiency carrier recover DPSK , clock recovery , Probability of error and bit error rate.

UNIT II
Data Communications ; Serial , Parallel configuration , Topology , Transmission modes , codes , Error Control Synchronization, LCU.

UNIT III
Serial and Parallel Interfaces , Telephone Networks and Circuits , Data modems

UNIT IV
Data Communication Protocols , Character and block Mode ,Asynchronous and Synchronous Protocols, public Da Networks , ISDN.

UNIT V
LOCAL AREA NETWORKS : token ring , Ethernet , Traditional , Fast and GIGA bit Ethernet, FDDI

UNIT VI
DIGITAL MULTIPLEXING : TDM , T1 carrier , CCITT , CODECS, COMBO CHIPS , North American Hierarchy , Line Encoding , T-carrier , Frame Synchronization Inter Leaving Statistical TDM FDM , Hierarchy ,Wave Division Multiplexing .

UNIT VII
WIRELESS LANS
IEEE 802.11 Architecture Layers , Addressing, Blue Tooth Architecture Layers, l2 Cap , Other Upper Layers .

UNIT VIII
MULTI MEDIA
Digitalizing Video and Audio Compression Streaming Stored and Live Video and Audio , Real Time Interactive Video and Audio , VOIP

TEXT BOOKS
1. Electronic communication systems , fundamentals through advanced - W. TOMASI ,Pearson 4th Edition
2. Data communication and networking - B.A. Forouzen

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I - Semester

ALGORITHM ANALYSIS AND DESIGN
(ELECTIVE- II)

UNIT I

Algorithm definitions, correctness time and space complexity, average and worst case analysis, optimality, P and NP complete problems.

UNIT II

Algorithmic languages and data structures. Numerical and non-numerical, combinational and log algorithms, Polynomial metrics, and vector manipulations.

UNIT III

FFT and Signal processing algorithms, algorithms for linear and non-linear, integer and dynamic programming problems.

UNIT IV

Searching, Sorting, merging sorted listed, string matching, trees, decision trees, game trees, branch and bound algorithms.

UNIT V

Set representation and components of a graph, shortest path problems, traveling salesman problem, parallel algorithms and distributed processing NP complete algorithms.

SUGGESTED READING

1. Horowitz E Sahni S and Sanguthevar Rajasekaran: "Fundamental of Computer Algorithms", Galgotia Publications, 2001.
2. Aho, A.U. Hopcraft JV, Ullman J.D : The design and analysis of Computer Algorithms, Addison Wesley Pub.Co., 1974.
3. Gillis Branard and Paul Bratley: Fundamentals of Algorithms, Prentice Hall, 1996.
4. Corness, Leiserson, Rivest, "Algorithms" Pearson Publication, 2002.
5. Goodman, intro to the Design & Analysis of Algorithams TMH

I - Semester

IMAGE AND VIDEO PROCESSING
(ELECTIVE - II)

UNIT 1

Fundamentals steps of Image processing, Components of an Image processing system, Image sampling and quantization, relationship between the pixels. Gray level transformation, Histogram processing, Smoothing and sharpening spatial filters, Smoothing and sharpening frequency domain filters, Homomorphic filtering Restoration filters – spatial and frequency domain, Inverse filter, Wiener filter

Color image processing : Pseudocolor image processing, Color transformation, Smoothing and sharpening

UNIT 2

Morphological operations: Dilation and erosion, Opening and closing, Hit or Miss transforms, Morphological algorithms, Extensions to gray scales images and its applications.

Image compression: Compression models, Error free coding, lossy coding, compression standards, color image compression

Image segmentation : Edge linking and boundary detection, Thresholding, Region based segmentation, Segmentation by morphological watersheds, color segmentation

UNIT 3

Video formation, perception and representation: Color perception and specification, Video capture and display, Analog video raster, Analog color TV systems, Digital Video

Video Sampling: Basics of lattice theory, sampling over lattice, Sampling of video signals, filtering operations, Conversion of signals sampled on different lattices, Sampling rate conversion of video signals

UNIT 4

Video modeling : Camera model, illumination model, object model. Scene model, Two dimensional motion models

2-D motion estimation: Optical flow, General methodologies, Pixel based mtion estimation, Block matching algorithm, Mesh-based motion estimation , Global motion estimation, Region based motion estimation, Multiresolution motion estimation. Application of motion estimation in video coding

UNIT 5

Video coding: Information theory, Binary encoding, Scalar quantization, Vector quantization, Waveform based video coding: Block based transform coding, Predictive coding, Object based scalability, Wavelet Transform based coding

REFERENCE BOOKS

1. Digital Image processing – Gonzaleze and woods
2. Video processing and communication – Yao Wang, Joern Ostermann and Ya-Qin Zhang, Prenticd Hall
3. Digital video processing – M. Tekalp

I Semester

HDL SIMULATION LABORATORY

Note: i. All the experiments are to be carried out independently by each student, with different specifications.

ii. Atleast 15 experiments are to be carried out.

1. Experiments using VERILOG HDL Simulation and timing analysis on
   a. The Design of Digital Building Blocks for Combinational Circuits (4 to 6-MSI)
   b. The Design of Sequential Circuits (6 to 8-MSI & 1 or 2-VLSI Circuits) for.
2. Experiments using micro controllers tools
3. 2 to 3 Mini projects on Digital/Mixed Design (VHD/Verilog) Incorporating Optimization techniques.

II - Semester

REAL TIME OPERATING SYSTEMS FOR EMBEDDED SYSTEMS

UNIT –1:
Introduction to Unix, Overview of commands, File I/O. (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Signals, Interprocess Communication (pipes, fifos, message queues, semaphores, shared memory).

UNIT – 2:
Real Time Systems: Typical real time application, Hard Vs soft real time systems, A reference model of Real Time Systems: Processors and resources, Temporal parameters of Real time workload, periodic task model, precedence constraints and data dependency functional parameters, Resource parameters of jobs and parameters of resources. Commonly used approaches to Real Time Scheduling: Clock driven, Weighted Round Robin, priority driven, Dynamic Vs State Systems, Effective release times and Dead lines, offline Vs online scheduling.

UNIT – 3:
Operating Systems : Overview, Time Services and Scheduling mechanisms, other basic operating system function, processor reserves and resource kernel. Capabilities of commercial Real time Operating Systems.

UNIT – 4:
Fault Tolerance Techniques: Introduction, Fault causes, Types, Detection, Fault and error containment, Redundancy: Hardware, Software, Time. Integrated Failure handling.

UNIT – 5:
Case Studies: VX works: Memory Managements task state transiton diagram, pre-emptive priority, scheduling, context switches – semaphore – Binary mutex, Counting: watch dugs, I/O System
RT Linux: Process Management, scheduling, Interrupt management, and synchronization

SUGGESTED BOOKS

1. Advanced Unix Programming – Richard Stevens
2. Real Time Systems – Jane W.S. Liu - Pearson Education
3. Real Time Systems – C.M.Krishna, KANG G. Shin – M.G.Hill
4. VxWorks Programmers Guide

www.tidp.org

www.kernel.org

http://www.xml.com/ldd/chapter/book

II Semester

DSP PROCESSORS AND ARCHITECTURES

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV

EXECUTION CONTROL AND PIPELINING.

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT VI

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT VII

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

II Semester

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

UNIT I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cypres FLASH 370 Device Technology, Lattice pLSI's Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping jfor FPGAs, Case studies – Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and their speed performance.

UNIT III

Finite State Machines (FSM): Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL. Alternative realization for state machine chart suing microprogramming. Linked state machines. One – Hot state machine, Petrinetes for state machines – basic concepts, properties. Extended petrinetes for parallel controllers.

Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT IV

FSM Architectures and Systems Level Design: Architectures centered around non-registered PLDs. State machine designs centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT V

Digital Front End Digital Design Tools for FPOGAs & ASICs: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of paraller adder cell, paraller adder sequential circuits, counters, multiplexers, parallel controllers.

SUGGESTED BOOKS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publicatgions, 1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.

II - Semester

EMBEDDED SOFTWARE DESIGN

UNIT 1

Pentium Processor: Introduction to the Pentium Microprocessor, Special Pentium Registers, Pentium Memory management.

UNIT 2

Embedded Design Life Cycle: Introduction, Product Specification, Hardware/software partitioning, Iteration and Implementation, Detailed hardware and software design, Hardware/Software integration, Product Testing and Release, Maintaining and upgrading existing products. Selection Process: Packaging the Silicon, Adequate Performance, RTOS Availability, Tool chain Availability, Other issues in the Selection process, Partitioning decision : Hardware/Software Duality, Hardware Trends, ASICs and Revision Costs.

UNIT 3

Development Environment: The Execution Environment, Memory Organization, System Startup. Special Software Techniques: Manipulating the Hardware, Interrupts and Interrupt service Routines (ISRs), Watchdog Times, Flash Memory, Design Methodology. Basic Tool Set: Host – Based Debugging, Remote Debuggers and Debug Kernels, ROM Emulator, Logic Analyzer.

UNIT 4

BDM: Background Debug Mode, Joint Test Action Group (JTAG) and Nexus.
ICE – Integrated Solution: Bullet Proof Run Control, Real time trac, Hardware Break points, Overlay memory, Timing Constrains, Usage Issue, Setting the Trigger.
Testing: Why Test? When to Test? Which Test? When to Stop? Choosing Test cases, Testing Embedded Software, Performance Testing Maintenance and Testing, The Future.

UNIT 5

Writing Software for Embedded Systems: The compilation Process, Native Versus Cross-Compilers, Run-time Libraries, Writing a Library, Using alternative Libraries, using a standard Library, Porting Kernels, C extensions for Embedded Systems, Downloading. Emulation and debugging techniques; Buffering and Other Data Structures: What is a buffer? Linear Buffers, Directional Buffers, Double Buffering, Buffer Exchange, Linked Lists, FIFOs, Circular Buffers, Buffer Under run and Overrun, Allocating Buffer Memory, Memory Leakage. Memory and Performance Trade-offs

TEXTBOOKS

1. Intel Microporcessors by Barry B Brey PHI
2. Embedded System Design – Introduction to Processes, Tools, Techniques, Arnold S Burger, CMP Books
3. Embedded Systems Design by Steve Heath, Newnes

II - Semester

SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION (ELECTIVE - III)

UNIT I
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

UNIT II
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT III
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT IV
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT V
Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

SUGGESTED READING:

1. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, "Programming PERL", Oreilly Publications, 3rd Edn., 2000.
3. Tom Christiansen, Nathan Torkington, PERL Cookbook, Oreilly Publications, 3rd Edn,2000.

II Semester

LOW POWER VLSI DESIGN
(Elective III)

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

MOS/BiCMOS PROCESSES : Bi CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes ,SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT IV

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models.

UNIT V

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid-mode environment.

UNIT VI

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates. Performance evaluation

UNIT VII

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS Digital circuits. ESD-free Bi CMOS , Digital circuit operation and comparative Evaluation.

UNIT VIII

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip-flops, Design perspective.

TEXT BOOK:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES:

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996
2. CMOS Digital ICs sung-moKang and yusuf leblebici 3rd edition TMH 2003 (chapter 11)
3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

II Semester

ADVANCED DIGITAL FILTERING
(ELECTIVE – III)

UNIT I

Multirate Digital Signal Processing: Introduction – Decimation by integer factor, Interpolation by an integer factor. Sampling rate conversion by non-integer factors, Multistage approach to sampling rate conversion. Design of practical sampling-rate converters. Software implementation of interpolators and decimators. Sample rate conversion using polyphase filter structure. Examples of applications of multirate DSP.

UNIT II

Linear prediction and optimum linear filters: Representation of a stationary random process. Rational power spectra- A.R, M.A & ARMA processes. Relationship between the filter parameters and Auto-correlation sequence. Forward and Backward linear prediction. Optimum reflection coefficient for the Lattice forward and backward and backward predictors. A.R. process and linear prediction. Solution of Normal equations. Levinson-Durbin algorithm. The schur algorithm. Pipelined architecture for implementing the Schur algorithm. Properties of linear Prediction error filters. AR Lattice and ARMA Lattice-Ladder filters.

UNIT III

Adaptive Digital filters: Concepts, Basic weiner filter theory, Basic LMS adaptive algorithm, Recursive least squares algorithm, Application examples.

UNIT IV

Applications of Adaptive filters: Adaptive channel equalization, Echo cancellation in Data Transmission over Telephone channels, Adaptive noise canceling.

UNIT V

Recursive Least Squares Algorithms for array signal processing: QR Decomposition for least squares Estimation Gram – Schmidt orthogonalization for least squares Estimation, Estimation of spectra from finite – Duration observation of signals: Parametric and non parametric methods for power spectrum Estimation

REFERENCES

1. E.C.Ifeachor et.al., Digital Signal Processing, Pearson Education
2. John G.Proakis, C.M.Radar, Algorithms for statistical signal processing. Pearson Education.
3. Dimitirs G.Manolakis Statistical & Adaptive Signal Processing TMH.

II - Semester

DESIGN FOR TESTABILITY
(ELECTIVE - IV)

UNIT I

Introduction to Test and Design for Testability (DFT) Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scans standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT V

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Introduction to automatic in circuit testing (ICT), JTAG Testing features.

SUGGESTING READING

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
3. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

II - Semester

MICRO ELECTROMECHANICAL SYSTEMS
(ELECTIVE - IV)

UNIT I

Introduction, Basic Structures of MEM Devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of Micro Electromechanical Systems (MEMs) to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatability of MEMS from the point of Power Dissipation, Leakage etc.

UNIT II

Review of Mechanical Concepts like Stress, Strain, Bending Moment, Deflection Curve. Differential equations describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with voltage in C.L, Deflection Vs Voltage Curve, Critical Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT III

Two Terminal MEMS – capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures.

Three Terminal MEM structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

UNIT IV

MEM Circuits & Structures for Simple GATES – AND, OR, NAND, NOR, Exclusive OR< simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping.

RF Switches for Modulation.

MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT V

MEM Technologies: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers Etc., Etching Technologies.

Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

SUGGESTED BOOKS

1. Gabriel.M.Review, R.F. MEMS Theory, Design and Technology, John Wiley & Sons, 2003.
2. Strength of Materials – by Thimo Shenko, CBS Publishers & Distributors., 2000.
3. Ristic L. (Ed.) Sensor Technology and Devices, Artech House, London 1994.
4. Servey E.Lyshevski, MEMS and NEMS, Systems Devices; and Structures, CRC Press, 2002.

II Semester

WIRELESS COMMUNCIATIONS AND NETWORKS
(ELECTIVE IV)

UNIT I

WIRELESS COMMUNICATIONS & SYSTEM FUNDAMENTALS: Introduction to wireless communications systems, examples, comparisons & trends. Cellular concepts-frequency reuse, strategies, interference & system capacity, trucking & grade of service, improving coverage &capacity in cellular systems.

UNIT II

MULTIPLE ACCESS TECHNIQUES FOR WIRELESS COMMUNICATION: FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques),SDMA technique(AS applicable to wireless communications).Packet radio access-protocols, CSMA protocols ,reservation protocols ,capture effect in packet radio , capacity of cellular systems .

UNIT III

WIRELESS NETWORKING: Introduction , differences in wireless & fixed telephone networks, traffic routing in wireless networks –circuit switching ,packet switching X.25 protocol.

UNIT IV

Wireless data services – cellular digital packet data(CDPD),advanced radio data information systems ,RAM mobile data (RMD). Common channel signaling (CCS),ISDN-Broad band ISDN & ATM ,Signaling System no .7(SS7)-protocols, network services part, user part, signaling traffic, services & performance.

UNIT V

MOBILE IP AND WIRELESS APPLICATION PROTOCOL: Mobile IP Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol.

UNIT VI

WIRELESS LAN TECHNOLOGY: Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs, IEEE 802 protocol Architecture, IEEE802 architecture and services, 802.11 medium access control, 802.11 physical layer.

UNIT VII

BLUE TOOTH : Overview, Radio specification, Base band specification, Links manager specification, Logical link control and adaptation protocol. Introduction to WLL Technology.

UNIT VIII

MOBILE DATA NETWORKS : Introduction, Data oriented CDPD Network, GPRS and higher data rates, Short messaging service in GSM, Mobile application protocol.

TEXTBOOKS

1. Wireless Communication and Networking – William Stallings, PHI, 2003.
2. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, PHI, 2nd Edn., 2002.
3. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, Pearson Education, 2002.

REFERENCES

1. Wireless Digital Communications – Kamilo Feher, PHI, 1999.

II - Semester

FPGA SYNTHESIS LABORATORY

Note: i. All the experiments are to be carried out independently by each student, with different specifications

ii. At least 15 experiments are to be carried out.

1. Synthesis of the designs made using "VHDL / VERILOG and Mixed Design (VHDL & Verilog)" after Simulation are to be verified using FPGA/CPLD blocks from different commercially available products on:

   i. Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
   ii. Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

2. Experiments on Digital Signal Processors.

3. Mini projects on RTOS

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