

COURSE STRUCTURE
AND
DETAILED SYLLABUS

M.TECH
EMBEDDED SYSTEMS & VLSI DESIGN
(EFFECTIVE FOR THE STUDENTS ADMITTED FROM THE ACADEMIC –
YEAR 2008 -09)

COURSE STRUCTURE AND SYLLABUS

Course No.	Subject	Contact Hours/Week
FIRST SEMESTER	Micro Controllers for Embedded System Design	4
	Analog and Digital IC design	4
	Embedded Systems Concepts	4
	VHDL Modelling of Digital Systems	4
Elective-I	Modelling and Synthesis with Verilog HDL	4
	Hardware Software Co-design	
	Low Power VLSI Design	
Elective-II	RF and Microwave Integrated Circuits	4
	Micro Electromechanical Systems	
	Embedded Software design	
LAB:	HDL Programming and VLSI Design Lab	3
SECOND SEMESTER	VLSI Technology and Design	4
	Real Time Operating Systems for Embedded Systems	4
	DSP Processors and Architectures	4
	CPLD and FPGA Architecture and Applications	4
Elective-III	Design for Testability	4
	Algorithms for VLSI Design Automation	
	Network Security and Cryptography	
Elective-IV	Image and Video Processing	4
	Scripting Language for VLSI Design Automation	
	Advanced Digital Filtering	
LAB:	Embedded Systems Design Lab	3
THIRD & FOURTH SEMESTER	Seminar and Project	

MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT -I

INTRODUCTION TO EMBEDDED SYSTEMS

Review of micro controllers and their features. 8 & 16 bit Micro Controller Families (of Intel 8051) Flash Series. Motorola 68 HC II: Micro Chip PIC 16C6X and Micro controller hardware. Embedded RISC Processor Architectures ARM6TDMI (Advanced RISC Machine).

UNIT -II

MICRO CONTROLLER INTERFACING

8051. 68GC II: PIC-16C6X and ATMEL External Memory Interfacing- Memory Management Unit. Instruction and data cache, Memory controller. On chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, LAP features.

UNIT -III

PROGRAMMING

Instruction sets and Assembly language Programming concepts and programming the 8051, 68HC11, PIC 16C6X Micro controller, ARM6TDMI Core(SoC) and PIC-IDE.

UNIT -IV

Interrupt synchronization – Interrupt vectors & Priority, External interrupt design. Serial I/O devices, RS232 Specifications, RS422/Apple Talk/RS423/RS436 & Other communication protocols. Serial Communication Controller.

UNIT -V

Ethernet Protocol, SDMA, Channels and IDMA simulation, CPM interrupt controller and CPM Timers. Power controls. External BUS interface system development and debugging.

CASE STUDIES: Design of embedded systems using the micro controller– 8051/ARM6TDMI, for applications in the area of Communications, Automotives, Industrial control.

SUGGESTED BOOKS

1. M.A. Mazadi & J.G. Mazidi, "the 8051 Micro controller Embedded Systems" Pearson Education, Asia(2002)
2. John B. Peatman, Designing with PIC Micro Controllers, Pearson Education
3. Jonathan W. Valnano, Embedded microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning 1999.
4. Cathey may and Silha (Ed). " The power PC Architecture" Morgan Kauffman Press, (1998).

ANALOG AND DIGITAL IC DESIGN

UNIT -1

OPERATIONAL AMPLIFIERS : General considerations, one-stage op-amps. Two stage op-amps gain boosting stage – comparison, I/P range limitations, slew rate.

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: simple CMOS. , BJT current mirrors, Cascode Wilson Wilder current mirrors. Common source amplifier, source follower, common gate amplifier.

NOISE: Types of Noise – Thermal Noise – flicker noise – Noise in Op-amps – Noise in common source stage, Noise band width.

UNIT – II

PHASE LOCKED LOOP DESIGN: PLL concepts – The phase locked loop in the locked condition, Intergrated circuit PLLs - Phase Detector – Voltage controlled oscillator – case study : Analysis of the 560 B Monolithic PLL.

SWITCHED CAPACITOR CIRCUIT : Basic Building blocks, Op-amps, capacitor switches, non-overlapping clocks – Basic operations and analysis– resistor equivalence of a switched capacitor, parasitic sensitive integrator, parasitic insensitive integrators, signal flow graph analysis. First order filters – switch sharing, Fully differential filters – charged injections – switched capacitor –gain circuits, parallel resistor – capacitor circuit – presettable gain circuits –other switched capacitor circuits–full wave rectifier peak detector – sinusoidal oscillator.

UNIT – III

LOGIC FAMILIES & CHARACTERISTICS : CMOS, TTL, ECL, logic families, CMOS, TTL, interfacing, comparison of logic families.

COMBINATIONAL LOGIC DESIGN USING VHDL: VHDL modeling for decoders, encoders, multiplexers, comparators, adders and subtractors.

SEQUENTIAL IC DESIGN USING VHDL: modeling for latches, flip flops, counters, shift registers, FSMs.

UNIT – IV

DIGITAL INTEGRATED SYSTEM BUILDING BLOCKS: Multiplexers and decoders -Barrel shifters, counters, digital single bit adder.

MEMORIES: ROM : Internal structure, 2D decoding, commercial types, timing and applications.

CPLD: XC 9500 series family CPLD architecture, functional block internal architecture, I/O block internal structure.

FPGA: Conceptual view of FPGA-classification based on CLB arrangement, Programming technologies-XC 4000 series family architecture-CLB internal architecture –I/O block architecture.

UNIT V

COMPARATORS: Using an Op-amp for a comparator-charge injection errors-latched comparator.

NYQUIST RATE D/A converters: Decoder based converter resistor string converters, folded resistor string converter –Binary scale converters- Binary weighted resistor converters, reduced resistance ratio ladders-R-2R based converters-Thermometer code current mode D/A converters.

NYQUIST RATE A/D converters: Integrating converters – successive approximation converters - DAC based successive approximation – flash converters, time interleaved A/D Converters.

REFERENCES

1. Analog Integrated Circuit Design by David A. Johns. Ken Martin, John Wiley & Sons.
2. Analysis and Design of Analog Integrated Circuits by Gray, Hurst Lewis, Meyer, John Wiley & Sons.
3. Design of Analog CMOS Integrated Circuits. Behzad Razavi. TMH
4. Digital Integrated Circuit Design by Ken Martin. Oxford University 2000
5. Digital Design Principles & Practices by John F Walkerly, Pearson Education & Xilinx Design Series. 3rd Ed.(2002)

SUGGESTING READING

1. Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis" Prentice Hall, India (2002)
2. Douglas J Smith "HDL Chip Design, a Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs using VHDL or Verilog, Doone Publications (1999).

EMBEDDED SYSTEMS CONCEPTS

UNIT – I

AN INTRODUCTION TO EMBEDDED SYSTEMS

An Embedded system, Processor in the system, other hardware units, software embedded into systems, Exemplary embedded system, Embedded System On – Chip (SoC) and in VLSI circuit, Processor and memory organization – structural units in a processor, Processor selection for an Embedded system, Memory devices, memory selection for an Embedded system, allocation of memory to program cache and memory management links. Segments and blocks and memory map of a system. DMA, Interfacing processors, Memories and Input Output devices.

UNIT – II

DEVICES AND BUSES FOR DEVICE NETWORKS

I/O devices, timer and counting devices, Serial communication using the “12C” CAN, Profibus Foundation field bus, and advanced I/O buses between the network multiple devices, host systems or computer parallel communication between the networked I/O Multiple devices using the ISA,PCI, PCI-X and advanced buses.

UNIT – III

DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM

Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism.

UNIT – IV

PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C,C++, VC++ AND JAVA

Interprocess communication and synchronization of processes, task and threads, multiple processes in an application, problem of sharing data by multiple tasks and routines, interprocess communication.

UNIT – V

HARDWARE - Software co-design in an Embedded system, Embedded system project management, Embedded system design and co- design issues in system development process. Design cycle in the development phase for an Embedded system, use of target systems. Use of software tools for development of an embedded system, use of scopes and logic analysis for system, hardware tests. Issues in embedded system design.

TEXT BOOK

1. Embedded system: Architecture, Programming and Design by Rajkamal, TMH

REFERENCE

1. Embedded system design by Arnold Burger, CMP
2. An embedded software Primer, by David Simon, PEA
3. Embedded system design: Real world design, by Steve Heath: Butterworth Heinenann. Newton mass USA 2002
4. Data communication by Hayt.

II – Semester

VHDL MODELLING OF DIGITAL SYSTEMS

UNIT – I

INTRODUCTION:

An Overview of Design procedures used for system design using CAD tools. Design entry, Synthesis simulation, Optimization, Place and Route. Design Verification tools, Examples using commercial PC based on VHDL elements of VHDL top down design with VHDL subprograms . Controller description VHDL operators.

UNIT – II

BASIC CONCEPTS IN VHDL:

Characterizing Hardware Languages, Objects and Classes, Signal assignments, Concurrent and Sequential assignments. Structural specification of hardware : parts library wiring of primitives, wiring interactive networks, modeling a test bench binding alternative up down wiring.

UNIT – III

DESIGN ORGANIZATION AND PARAMETERIZATION:

Definition and usage of subprograms, Packaging parts and utilities, Design parameterization, Design configuration, Design libraries, Utilities for high level descriptions, type declaration and usage. VHDL operators, subprogram parameter types and overloading, Other types and type related issues, predefined attributes, user defined attributes, packing basic utilities.

UNIT –IV

DATA FLOW DESCRIPTION IN VHDL

Multiplexing and data selection, State machine description, Open collector gates, here state bussing A general data flow circuit, Updating basic utilities, Behavioral description of hardware process statement, Assertion statements, Sequential wait statements, formatted ASCII I/O operators, MSI-based design.

UNIT –V

CPU MODELLING FOR DESCRIPTION IN VHDL:

Parawan CPU, Behavioural description of parawan, Bussing structure, Data flow description, Test bench for the parawan CPU, A more realistic parawan. Interface design and modeling, VHDL as a modeling language.

TEXT BOOKS:

1. ZNAWABI : VHDL analysis and modeling of digital systems (2/E) McGraw Hill. (1998)

REFERENCE:

- 1.PERRY : VHDL .(3/E) McGraw Hill

I – Semester**MODELING AND SYNTHESIS WITH VERILOG HDL**
(ELECTIVE – I)**UNIT – I****HARDWARE MODELING WITH THE VERILOG HDL:**

Hardware encapsulation – the verilog module, hardware modeling verilog primitives. Descriptive styles, Structural connections, Behavioral description in Verilog, hierarchical descriptions of hardware, Structured (top down) design methodology, Arrays of instances, Using verilog for Synthesis, Language conventions, representation of numbers.

UNIT – II**LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL**

User defined primitives–combinational behavior user–defined primitives, Sequential behavior, Initialization of sequential primitives. Verilog variables, logic value set data types, strings. Constants, Operators, Expressions and Operands, operator precedence, models of propagation delay, built in constructs for delay signal transitions, verilog models for gate propagation delay (Interial delay), time scales for simulation, verilog models for net delay (Transport delay), module paths and delays, path delays and simulation, interial delay effects and pulse rejection.

UNIT – III**BEHAVIORAL DESCRIPTIONS IN VERILOG HDL:**

Verilog behaviors, Behavioral statements, Procedural assignment, Procedural continuous assignments, Procedural timing controls and synchronization, Intra- assignment, delay–blocked assignments, non blocking assignment, intra assignment delay, Non blocking assignment, Simulation of simultaneous procedural assignments, repeated intra assignment Delay, indeterminate assignments and ambiguity constructs for activity flow control, tasks and functions, Summary of delay constructs in Verilog system, Tasks for timing checks, Variable scope revisited Module contents, Behavioral models of finite state machines.

UNIT – IV**SYNTHESIS OF COMBINATIONAL LOGIC:**

HDL- based synthesis, technology independent design benefits of synthesis, Synthesis methodology, vendor support, styles for synthesis of combinational logic, technology mapping and shared resources, three state buffers, three state outputs and don't cares, Synthesis of sequential logic, Synthesis of sequential udps, Synthesis of latches, synthesis of edge triggered flip flops registered combinational logic, shift registers and counters, Synthesis of finite state machines resets, synthesis of gated clocks, Design partitions and hierarchical structures.

UNIT – V**SYNTHESIS OF LANGUAGE CONSTRUCTS:**

Synthesis of nets, Synthesis of register variables, Restrictions on synthesis of "X" and "Z", Synthesis of expressions and operators, Synthesis of assignments, synthesis of case and conditional statement. Synthesis of Resets, Timings controls in Synthesis, Synthesis of multi cycle operations, Synthesis of loops, synthesis of fork join blocks, Synthesis of the disable statement. Synthesis of user defined

tasks, Synthesis of user defined functions. Synthesis of specify blocks. Synthesis of compiler directives, Switch level models in verilog, MOS transistor technology, switch level models of MOS transistors, Switch level models of static CMOS circuits, Alternative loads and pull gates, CMOS transmission gates. Bi-directional gates (switches), signal strengths, and wired logic. Design examples in verilog.

TEXT BOOK

1. M.D.CILETTI : Modeling synthesis and rapid prototyping with the verilog HDL (1999) PRENTICE – Hall.

REFERENCE

M.G ARNOLD : Verilog digital computer design (1999) Prentice – Hall (ptr)

I – Semester

HARDWARE – SOFTWARE CO – DESIGN **(ELECTIVE – I)**

UNIT I

CO- DESIGN ISSUES AND CO- SYNTHESIS ALGORITHMS:

Co- Design Models: Architectures, languages, a generic co- design methodology, Hardware software synthesis algorithms: hardware – software partitioning, distributed system co- synthesis.

UNIT – II

PROTOTYPING AND EMULATION AND TARGET ARCHITECTURES:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture, specialization techniques. System communication infrastructure, target architectures and application system classes, architectures for control dominated system and data – dominated systems.

UNIT –III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES :

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT – IV

DESIGN SPECIFICATION AND VERIFICATION :

Design, co-design, the co-design computational model, concurrency, coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT - V

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN :

System – level specification, design representation for system level synthesis. System Level specification languages, heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS :

1. Hardware / Software co-design principles and practice, Kluwer academic publishers

I – Semester

LOW POWER VLSI DESIGN
(ELECTIVE – I)

UNIT – I

LOW POWER DESIGN, AN OVER VIEW : Introduction to low – voltage low power design, limitations, silicon –on-Insulator

UNIT – II

MOS/BiCMOS PROCESSES : Bi CMOS Processes, Integration and Isolation considerations, Integrated Analog/ Digital CMOS Process.

UNIT - III

LOW –VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES : Deep submicron processes, SOI CMOS, Lateral BJT on SOI, future trends and directions of CMOS/BICMOS processes.

UNIT – IV

DEVICE BEHAVIOR AND MODELING : Advanced MOSFET models, limitations of MOSFET models, Bipolar models.

UNIT – V

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybridmode environment.

UNIT -VI

CMOS AND Bi –CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates. Performance evaluation.

UNIT – VII

LOW –VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS digital Circuits, ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT – VIII

LOW POWER LATCHES AND FLIP FLOPS : Evolution of latches and flip flops-quality measures for latches and flip flops. Design perspective.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low viltage, low power by Yeo Rofail/Gohl(3 authors), Pearson Education Asia, 1st Indian reprint, 2002.

REFERENCES

1. Digital Integrated circuits, J.Rabaey, PH.N.J 1996
2. CMOS Digital ICs, Sung-Mokang and Yusuf Ieblebici, 3rd edition, TMH 2003 (chapter II)
3. VLSI DSP Systems, Parhi, John Wiley & Sons, 2003 (chapter 17)

4.I EEE Trans Electron Devices, IEEE J.Solid State Circuits and other National and International Conferences and Symposia.

M.Tech (Embedded Systems & VLSI Design)

W.e.f.2008 -09

I – Semester

R.F AND MICROWAVE INTEGRATED CIRCUITS

(ELECTIVE –II)

UNIT –I

Analysis and design of RF and microwave lines, Review of transmission lines, parallel plate transmission line, low frequency solution, strip line and micro strip transmission lines, low frequency solution, high frequency properties of microslot line, coplanar wave guides, coupled microstrip lines, spiral inductors, capacitors.

UNIT – II

Microstrip / Stripline based filters. Resonators, phase shifters, micro based gyrators, circulators and isolators, directional couplers.

UNIT – III

Microwave active devices – microwave transistors, GaAs FETS (Structures, equivalent circuits). Low noise amplifiers. Power amplifiers, oscillators, detectors, mixers, modulators and switches.

UNIT – IV

Technology of MICS : Deposition techniques ,vacuum evaporation, vacuum sputtering, ion plating MBE (Molecular Beam Epitaxy) ,photo lithography, mask preparation, thick film technology, GaAs technology

UNIT – V

MIC packaging: Component attachment, bonding techniques, Solder reflow techniques, input/output terminations, testing.

SUGGESTED BOOKS:

1. I kneppo and J. Fabian, "Microwave Integrated Circuits" , London : Chapman & Hall (1994)
2. M.W Medley, "Microwave and RF circuit: Analysis, Synthesis and Design: Artech House (1993)
3. R.Goyal, "Monolithic Microwave Integrated Circuits: Technology & Design" Artech House (1998)
4. Y.Konishi, "Microwave Intergrated Circuits " Dekker , New York: Marcel Dekker,(1991)

I – Semester

MICRO ELECTROMECHANICAL SYSTEMS
(ELECTIVE –II)

UNIT –I

Introduction, basic structures of MEM devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.), Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT –II

Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, distributed force, deflection curves for canti levers – fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – transient response of the MEMS.

UNIT – III

Two terminal MEMS - capacitance Vs voltage Curve – variable capacitor. Applications of variable capacitors. Two terminal MEM structures.
Three terminal MEM structures – controlled variable capacitors – MEM as a switch and possible applications.

UNIT – IV

MEM circuits & structures for simple GATES – AND, OR, NAND, NOR, Exclusive OR, simple MEM configurations for flip-flops, triggering applications to counters, converters, Applications for analog circuits like frequency converters, wave shaping.
RF Switches for modulations. MEM Transducers for pressure, force temperature. Optical MEMS.

UNIT –V

MEM Technologies : silicon based MEMS – process flow – brief account of various processes and layers like fixed layer, moving layers, spacers etc. etching technologies.
Metal Based MEMS : Thin and thick film technologies for MEMS. PROCESS flow and description of the processes. Status of MEMS in the current electronics scenario.

SUGGESTED BOOKS

1. GABRIEL. M. Review, R.F. MEMS theory, Design and Technology. John wiley & Sons.2003.
2. Strength of Materials – by Thimo shenko, CBS publishers & Distributors.,2000.
3. Ristic (Ed) sensor technology and Devices, Artech House; London 1994.
4. Servey E.Lyshevski, MEMS and NEMS , systems Devices ;and structures, CRC press. 2002.

I- Semester

EMBEDDED SOFTWARE DESIGN **(ELECTIVE – II)**

UNIT - I

Pentium processor : introduction to the Pentium microprocessor, special Pentium registers, Pentium memory management.

UNIT – II

Embedded Design life cycle : Introduction, product specification, hardware / Software partitioning, iteration and implementation, detailed hardware and software design, Hardware/software integration, product testing and release, maintaining and upgrading existing products. Selection process : packaging the silicon adequate performance, RTOS availability, tool chain availability, other issues in the selection process, partitioning decision: hardware/ software duality, hardware trends, ASICs and revision costs.

UNIT – III

Development environment : The execution environment, memory organization, system startup, special software techniques : manipulating the hardware, interrupts and interrupt service routines (ISRs), watchdog times, flash memory design methodology, basic tool set: Host based debugging ,remote debuggers and debug kernels, ROM emulator, Logic analyzer.

UNIT – IV

BDM : Background debug mode, Joint Test Action Group (JTAG) and Nexus.

ICE- integrated solution : bullet proof run control, real time trac, hardware break points, Overlay memory, timing constraints, usage issue , setting the trigger.

Testing : why test? When to test? Which Test? When to stop? Choosing test cases, testing embedded software, performance testing ,maintenance and testing, the future.

UNIT –V

Writing software for embedded systems: the compilation process, Native versus Cross compliers, Runtime libraries, writing a library, using alternative libraries, using a standard library, proting kemels, extensions for embedded systems, Downloading. Emulation and debugging techniques : buffering and other data structures, what is a buffer? Linear buffers, directional buffers, double buffering, buffer exchange, linked list, FIFOs, circular buffers, buffer under run and overrun, allocating buffer memory, memory leakage, memory and performance trade – offs.

TEXT BOOKS

1. Intel microprocessors by Barry B Brey PHI
2. Embedded system Design _ Introduction to processes, tools, techniques, Arnold S Burger, CMP books.
3. Embedded systems design by Steve Heath, newness.

I – Semester

HDL PROGRAMMING AND VLSI DESIGN LABORATORY

1. Digital Circuits Description using Verilog
2. Verification of the functionality of designed circuits using function simulator
3. Timing simulation for critical path time calculation
4. Synthesis of digital circuits
5. Place and route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc
6. Implementation of designed digital circuits using FPGA and CPLD devices
7. MOS inverter DC characteristics, AC characteristics, transient analysis,
8. NMOS Characteristics
9. PMOS Characteristics
10. Layout basics – INV 1X, INV 2X, INV 4x INV 8X, NAND2, NOR2, EXOR, EXNOR.
11. Layout of adder, subtractor, multiplier.
12. Layout of comparator.
13. Advanced layout LNA, PLL, modulators, demodulators

Note: For experiments of 10,11,12 & 13 Items mentioned above: draw the schematics, perform simulation, extract the layout, run physical verification (DRC,LVS PEX) and post layout simulation.

II – Semester

VLSI TECHNOLOGY & DESIGN

UNIT – I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES : (MOS, CMOS, BiCMOS) Technology trends and projections.

UNIT – II

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICMOS CIRCUITS : I_{ds} - V_{ds} relationships, threshold voltage V_t , G_m , G_{ds} , G_{ds} and W_o , pass transistor, MOS, CMOS & BiCMOS inverters, Z_{pu} / Z_{pd} , MOS transistor circuit model, latch – up in CMOS circuits.

UNIT – III

LAYOUT DESIGN AND TOOLS : Transistor structures, Wires and Vias, Scalable design rules, Layout design tools.

UNIT – IV

LOGIC GATES & LAYOUTS : Static complementary gates, Switch logic, Alternative gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – V

COMBINATIONAL LOGIC NETWORKS : Layouts, Simulation, Network delay interconnect Design power optimization, Switch logic networks, gate and network testing.

UNIT – VI

SEQUENTIAL SYSTEMS : Memory cell, and Arrays, Clocking disciplines, Design power optimization, design validation and testing.

UNIT – VII

FLOOR PLANNING & ARCHITECTURE DESIGN : Floor planning methods, off-chip connections, high level synthesis, Architecture for low power SOCs and Embedded CPUs, Architecture testing.

UNIT – VIII

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN : Layout synthesis and Analysis, Scheduling and printing : Hardware/Software Co-design, chip design methodologies A simple Design example.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K Eshraghian et.al (3 authors), PHI of India Ltd., 2005
2. Modern VLSI Design, 3rd edition, Wayne Wolf, Pearson Education, fifth Indian reprint, 2005

REFERENCES:

1. Principles of CMOS design - N.H.E Weste, K.Eshraghain, Addison Wesley, 2nd edition
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990
3. CMOS Circuit Design layout and simulation – Baker, Li Boyce, PHI,2004.

II – Semester

REAL TIME OPERATING SYSTEMS FOR EMBEDDED SYSTEMS

UNIT – I

Introduction to Unix: Overview of commands, file I/O, (open, create,close, iseeek, read, write), process control (fork,vfork, exit,wait, waitpid, exec), signals, Interprocess communication (pipes, fifos, *message queues, semaphores, shared memory*).

UNIT – II

Real Time systems : typical real time applications, Hard Vs Soft real time systems, A reference model of Real Time Systems : Processors and resources, temporal Parameters of Real Time Workload, periodic task model, precedence constraints and data dependency, functional parameters, Resource parameters of jobs and parameters of resources. Commonly used approaches to real time scheduling clock driven, weighted round robin, priority driven, approaches to Real Time Scheduling, clock driven, weighted Round Robin, priority driven, Dynamic Vs state systems, Effective release time and Dead line, Offline Vs online scheduling.

UNIT – III

Operating systems : Overview, Time services and Scheduling mechanisms, other basic operating systems, function, processor reserves and resource kernel. Capabilities of commercial Real Time Operating Systems.

UNIT – IV

Fault Tolerance Techniques : Introduction, fault causes, Types, Detection, Fault and error containment, redundancy : Hardware, Software, Time. Integrated Failure handling.

UNIT – V

Case studies :VX works: Memory managements, task state transiton diagram, pre-emptive priority, scheduling context switches – semaphore –Binary mutex, counting watch dogs, I/O system, RT linux : Process management, Scheduling, Interrupt management, and Synchronization.

TEXT BOOKS

1. Advance Unix programming, Richard Stevens.
2. Real time systems – Jane W.S.Liu- Pearson education.
3. Real time system – C.M.Krishna, KANG G. shin –M.G.Hill.
4. Vx Works programmers Guide.

I I- Semester

DSP PROCESSORS AND ARCHITECTURES

UNIT – I

INTRODUCTION TO DIGITAL SIGNAL PROCESSING

Introduction, a digital signal – processing system, The sampling process, Discrete time sequences. Discrete fourier transform (DFT) and Fast fourier transform (FFT), Linear time invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP systems, MATLAB, DSP using MATLAB.

UNIT – II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic range and precision, source of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, Compensating filter.

UNIT – III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic architectural features, DSP computational building blocks, Bus architecture and memory data addressing capabilities, address generation unit, programmability and program execution, speed issues, Features for external interfacing.

UNIT – IV

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, relative branch support pipelining and performance, pipeline depth, Interlocking branching effects. Interrupt effects, pipeline programming models.

UNIT – V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial digital signal –processing devices, data addressing modes of TMS320C54XX DSPs. Data addressing modes of TMS320C54xx processors. Memory space of TMS 320C54XX processors, program control, TMS 320C54XX instructions and programming, On –chip peripherals, interrupts of TMS320C54XX processors, pipeline operation of TMS320C54XX processors.

UNIT –VI

IMPLEMENTATION OF BASIC DSP ALGORITHMS

The Q – notation, FIR filters, IIR filters, Interpolation filters, Decimation filters, PID controller, Adaptive filters, 2-D signal processing.

UNIT –VII

IMPLEMENTATION OF FFT ALGORITHMSAn FFT algorithm for DFT computation, A Butterly computation, Overflow and scaling, Bit – reversed index generation, An 8-point FFT implementation on the TMS 320C54XX, Computation of the signal spectrum.

UNIT – VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel Input/Output interface, Programmed I/O, Direct memory access (DMA)

A Multichannel buffered serial port (McBSP), McBSP programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital signal processing, Avtar Singh and S. Srinivasan, Thomson publications, 2004
2. DSP processor fundamentals, Architectures & features – Lapsley et al, S Chand & Co, 2000.

REFERENCES

1. Digital signal processors, Architecture, Programming and Applications – B. Venkata ramani and M Bhaskar, TMH, 2004
2. Digital signal processing - Jonathan Stein, John Wiley - 2005

II- Semester

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

UNIT – I

Programmable logic : ROM,PLA,PAL,PLD, PGA - features, programming and applications using complex programmable logic devices, Altera series – Max 5000/7000 series and Altera FLEX logic - 10000 series CPLD,AMDs, CPLD (Mach 1 to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures -3000 series, speed performance and in system programmability.

UNIT – II

FPGAs : field programmable gate arrays – logic blocks, routing architecture, design flow technology mapping for FPGAs, case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT -1,2,3 and their speed performance.

UNIT – III

Finite state machines (FSM), top down design, state transition table, state assignments for FPGAs, Problem of initial state assignment for one hot encoding. Derivations of state machine charges, Realization of state machine charts with a PAL .Alternative realization for state machine chart using microprogramming, linked state machine, One-hot state machine , petrinetes for state machines–basic concepts, properties, extended petrinetes for parallel controllers.

UNIT – IV

FSM Architectures and system level design: Architectures centered around non-registered PLDs, state machine designs centered around shift registers. One-hot design method. Use of ASM s in One-Hot design. K application of One-Hot method. System level design-controller, data path and functional partition.

UNIT –V

Digital front end digital design tools for FPGAs & ASICs : Using Mentor Graphics EDA tool ("FPGA Advantage ") – Design flow using FPGAs – Guidelines and case studies of parallel adder, cell parallel adder, sequential circuits, counters, multiplexers, parallel controllers.

SUGGESTED BOOKS:

1. PK Chan & S Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall (Pre).1994.
2. S.Trimberger, Edr., Field programmable gate array technology, Kluwer academic publications.1994.
3. J.old field, R.Dorf, Field Programmable Gate Arrays John- Wiley & Sons,Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer pubin,1992.

II – Semester

DESIGN FOR TESTABILITY (ELECTIVE – III)

UNIT – I

Introduction to test and design for testability (DFT) fundamentals.

Modeling: modeling digital circuits at logic level, register level and structural models, Levels or modeling

Logic simulations : Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT – II

Fault modeling – Logic faults models, fault detection and redundancy, fault equivalence and fault modeling-Logic fault models, fault detection and redundancy, fault equivalence and fault location. Signal struck and multiple struck – fault models. Fault simulation applications, general techniques for combinational circuits.

UNIT – III

Testing for single stuck faults (SSF), Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, functional testing with specific fault models. Vector simulation, ATPG vectors, formats, Compaction and compression, Selecting ATPG tool.

UNIT – IV

Design for testability –testability trade-offs, techniques, scan architectures and testing controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design board level and system level DFT approaches. Boundary scan standards. Compression techniques. Syndrome test and signature analysis.

UNIT – V

Built-In Self-Test (BIST) – BIST concepts and test pattern generation. Specific BIST ARCHITECTURES – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD ,SST, CATS, CSTP, PILBO . Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test types of memories and integration, Embedded memory testing model, Memory test requirements for MBIST, Brief ideas on Embedded Core testing.

Introduction to automatic in circuit testing (ICT),JTAG testing features.

SUGGESTED READING:

1. Miron Abramovici, Melvin A Breur, Arthur D.Friedman, Digital system testing and testable design, Jaico publishing house, 2001
2. Alfred Crouch, Design for test for Digital IC & Embedded Core systems, Prentice Hall
3. Robert J. Feugate, Jr.Steven M.Mentyn, Introduction to VLSI testing, Prentice Hall Englehood Cliffs. 1998.

II – Semester

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE – III)

UNIT - I

PRELIMINARIES:

Introduction to design methodologies, Design Automation tools, Algorithmic Graph theory, Computational complexity, tractable and intractable problems .

UNIT – II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION:

Backtracking branch and bound, Dynamic programming, Integer linear programming, Local search, simulated annealing, tabu search, Genetic Algorithms.

UNIT – III

Layout compaction, Placement, Floorplanning and Routing problems, Concepts and algorithms.

UNIT – IV

MODELLING AND SIMULATION : Gate level modeling and simulation, Switch level modeling and simulations.

UNIT – V

LOGIC SYNTHESIS AND VERIFICATION : Basic issues and terminology, Binary decision diagrams, two–level logic synthesis.

UNIT – VI

HIGH –LEVEL SYNTHESIS : Hardware models, Internal representation of the input algorithm, Allocation assignment and scheduling, some Scheduling Algorithms, some suspects of Assignment problem, High level transformations.

UNIT – VII

PHYSICAL DESIGN AUTOMATION OF FPGA TECHNOLOGIES, Physical design cycle for FPGAs, Partitioning and Routing for segmented and staggered models.

UNIT – VIII

PHYSICAL DESIGN AUTOMATION OF MCM TECHNOLOGIES, MCM physical design cycle, partitioning, placement – chip array based and full custom approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated pin–distribution and routing and programmable MCM's.

TEXT BOOKS:

1. Algorithms for VLSI design, S.H Gerez, WILEY student edition, John Wiley & Sons (Asia) pvt.Ltd.,1999.
2. Algorithms for VLSI physical design automation, 3rd edition, Naveed sherwani, springer international edition, 2005.

REFERENCES

1. Computer aided logical design with emphasis on VLSI-Hill & Peterson, Wiley, 1993
2. Modern VLSI design : systems on sillion – Wayne Wolf, Pearson education Asia, 2nd Edition, 1998.

NETWORK SECURITY AND CRYPTOGRAPHY
(ELECTIVE –III)

UNIT –I

INTRODUCTION : Attacks, Services and Mechanisms, Security attacks, Security services, A model for Internetwork security.

CLASSICAL TECHNIQUES : Conventional Encryption model, Steganography, Classical Encryption techniques.

UNIT – II

MODERN TECHNIQUES : Simplified DES, Block Cipher Principles, Data Encryption standard, strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations

ALGORITHMS : Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST – 128, RC2 characteristics of Advanced symmetric block ciphers.

UNIT – III

CONVENTIONAL ENCRYPTION : Placement of encryption function, Traffic confidentiality, key distribution, Random Number Generation.

PUBLIC KEY CRYPTOGRAPHY : Principles, RSA Algorithm, Key management. Diffie Hellman key exchange, Elliptic Curve Cryptography.

UNIT – IV

NUMBER THEORY : Prime and relatively prime numbers, modular arithmetic. Fermat's and Euler's theorems, Testing for primality, Euclid's algorithm, the Chinese remainder theorem, Discrete logarithms.

MESSAGE AUTHENTICATION AND HASH FUNCTIONS : Authentication requirements and functions, Message authentication, Hash functions, Security of Hash functions and MACs.

UNIT – V

HASH AND MAC ALGORITHMS : MD file, Message digest algorithm, Secure hash algorithm, RIPEMD – 160, HMAC.

DIGITAL SIGNATURES AND AUTHENTICATION PROTOCOLS : Digital signatures. Authentication protocols, digital signature standards.

UNIT – VI

AUTHENTICATION APPLICATIONS : Kerberos, X, 509 directory authentication service.

ELECTRONIC MAIL SECURITY : pretty good privacy, S/MIME.

UNIT – VII

IP SECURITY: Overview, Architecture, Authentication, Encapsulating security payload. Combining security associations, Key management.

WEB SECURITY: Web Security requirements , Secure sockets layer and Transport layer Security, Secure Electronic transaction.

UNIT – VIII

INTRUDERS, VIRUSES AND WORMS: Intruders, Viruses and related threats. Fire Walls : Fire Wall design principles, Trusted systems.

TEXT BOOKS

1. Cryptography and Net work security : Principles and Practice – William Stallings, Pearson Education .,2000.

II – Semester

IMAGE AND VIDEO PROCESSING (ELECTIVE – IV)

UNIT – I

Fundamentals, steps of Image Processing, Components of an Image processing system, Image Sampling and Quantization, relationship between the pixels. Gray level transformation, Histogram processing, Smoothing and sharpening spatial filters, Smoothing and Sharpening frequency domain filters, Homomorphic filtering, Restoration filters – spatial and frequency domain, inverse filter Wiener filter.

Color image processing : pseudo color image processing, color transformation, Smoothing and Sharpening.

UNIT – II

Morphological operations : Dilation and Erosion, Opening and Closing, Hit or Miss transforms, Morphological algorithms, Extensions to gray scale images and its applications.

Image compression : Compression models, Error free coding, lossy coding, Compression standards, color image compression.

Image Segmentation: Edge linking and Boundary detection, Thresholding, Region based segmentation. Segmentation by morphological watersheds, color segmentation.

UNIT – III

Video formation, perception and representation : Color perception and specification, Video capture and display , Analog video raster, Analog color TV systems, Digital video.

Video sampling: Basics of lattice theory, Sampling over lattice, Sampling of video signals, Filtering operations. Conversion of signals sampled on different lattice, Sampling rate conversion of Video signals.

UNIT – IV

Video modeling: Camera model, Illumination model, Object model, scene model, Two dimensional motion models.

2-D motion estimation : Optical flow, General methodologies, Pixel based motion estimation, Block matching algorithm, Mesh-based motion estimation, Global motion estimation, Region based motion estimation, Multiresolution motion estimation. Application of motion estimation in Video coding

UNIT – V

Video Coding : Information theory, Binary encoding, Scalar quantization, Vector quantization, Waveform based video coding. Block based transform coding, Predictive coding, Object based scalability , Wavelet transform based coding.

REFERENCE BOOKS

1. Digital Image Processing – Gonzalez and Woods

2. Video processing and Communication – Yao Wang, Joern Ostermann and Ya – Qin Zhang.
Prentice Hall.
3. Digital video processing – M.Tekalp.

II – Semester

SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION
(ELECTIVE – IV)

UNIT – I

Overview of Scripting Languages –PERL,CGI, VB Script, Java Script.

UNIT – II

PERL : Operators, Statements, Pattern matching etc, Data structures, Modules, Objects, Tied variables.

UNIT – III

Inter process Communication Threads, Compilation & Line Interfacing.

UNIT – IV

Debugger Internal & Externals, Portable Functions. Extensive exercises for programming in PERL.

UNIT –V

Other languages: Broad details of CGI, VB script, Java script with programming examples.

SUGGESTED READING:

1. Randal L; Schwartz Tom Phoenix, "Learning PERL" orcilly publications 3rd Edn.,2000.
2. Larry Wall, Tom Christiansen, John Orwant," Programming PERL," orcilly Publications, 3rd Edn.,2000.
3. Tom Christiansen, Nathan Torkington, PERL Cookbook, Orcilly publications, 3rd Edn, 2000.

II – Semester

ADVANCED DIGITAL FILTERING
(ELECTIVE – IV)

UNIT –I

Multirate digital signal processing : Introduction – Decimation by integer factor, Interpolation by an integer factor. Sampling rate conversion by non- integer factors, Multistage approach to sampling rate conversion. Design of practical sampling – rate converters. Software implementation of interpolators and decimators. Sample rate conversion using polyphase filter structure. Examples of applications of multirate DSP.

UNIT – II

Linear prediction and optimum linear filters : Representation of a stationary random process. Rational power spectra – A.R. M.A & ARMA processes. Relationship between the filter parameters and Auto – correlation sequence. Forward and Backward linear prediction, Optimum reflection coefficient for the lattice forward and backward predictors. A.R process and linear prediction, Solution of normal equations. Levinson-Durbin algorithm. The schur algorithm. Pipelined architecture for implementing the Schur algorithm. Properties of linear prediction error filters. AR Lattice and ARMA Lattice Ladder filters.

UNIT –III

Adaptive digital filters : Concepts, Basic wiener filter theory, Basic LMS adaptive algorithm. Recursive least squares Algorithm, Application examples.

UNIT – IV

Applications of Adaptive filters: Adaptive channel equalization, Echo cancellation in data transmission over telephone channels, Adaptive noise canceling.

UNIT – V

Recursive Least Squares Algorithms for array signal processing: QR Decomposition for least squares Estimation, Estimation of spectra from finite duration observation of signals: parametric and non parametric methods for power spectrum estimation.

REFERENCES

1. E.C I Feachor et.al., Digital signal processing, Pearson education.
2. John G.Proakis, C.M. Radar, Algorithms for statistical signal processing, Pearson Education.
3. Dimitirs G.Manolakis, Statistical & Adaptive signal processing, TMH.

II – Semester

EMBEDDED SYSTEMS DESIGN LAB

1. Study of Real time Operating Systems.
2. Development of Device Drivers for RT Linux.
3. Software Development for DSP Applications.
4. Serial Communication Driver for ARM processors.
5. LCD interface using 8051 microcontroller.
6. Keyboard / Display interface using M68HC11 controller.
7. Implementation of Timer/ Counter using PIC Microcontroller.
8. Case study:
 - (a) Microcontroller design tools.
 - (b) Design of RTOS Kernel.
 - (c) Cross compiler / Assembler.
 - (d) Vx Works.