JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

M.Tech (VLSI & Embedded Systems) *W.E.F 2007-08*

COURSE STRUCTURE AND SYLLABUS

Course No.	Subject	Contact Hours/week \
FIRST SEMESTER		
	Micro Controllers for Embedded System Design	4
	Analog and Digital IC Design	4
	Embedded System Concepts	4
	VHDL Modeling of Digital Systems	4
Elective-I		4
	Modelling and Synthesis with Verilog HDL	
	Hardware Software Co-Design	
	Low Power VLSI Design	
Elective – II		4
	RF and Microwave Integrated Circuits	
	Micro Electromechanical Systems	
	Embedded Software Design	
	HDL Programming & EDA Tools Laboratory	3
SECOND SEMESTER		
	VLSI Technology and Design	4
	Real Time operating systems for embedded systems	4
	DSP Processors & Architectures	4
	CPLD and FPGA Architecture and Applications	4
Elective-III		4
	Design for Testability	
	Algorithms for VLSI Design Automation	
	Network Security and Cryptography	
Elective –IV		4
	Image and Video Processing	
	Scripting Language for VLSI Design Automation	
	Advanced Digital Filtering	
	Embedded Systems Design Lab	3
THIRD & FOURTH SEMESTERS		
	SEMINAR	
	PROJECT	

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I-Semester

MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT –I
INTRODUCTION TO EMBEDDED SYSTEMS
Review of micro controllers and their Features. 8&16 Bit Micro Controller Families (Of Intel 8051) Flash Series, Motorola 68 HCII; Micro Chip PIC 16C6X and Micro controller hardware. Embedded RISC Processor Architectures – ARM6TDMI (Advanced RISC Machines).

UNIT –II
MICRO CONTROLLER INTERFACING
8051, 68GCII, PIC-16C6X and ATMEL External Memory Interfacing – Memory Management Unit, Instruction and data cache, Memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM. Watch dog, ISP. LAP features.

UNIT-III
PROGRAMMING
Instruction sets and assembly Ianguage Programme concepts and programming the 8051, 68HCII, PIC16C6X Micro controller ARM6TDMI Core (SOC) and PIC-IDE.

UINT – IV
Interrupt synchronization – Interrupt vectors & priority, external interrupt design. Serial I/O Devices RS232 Specifications, RS422/Apple Talk/ Rs 423/RS436 & other communication protocols. Serial communication controller.

UNIT – V
Ethernet Protocol, SDMA, Channels and IDMA Simulation, CPM Interrupt controller and CPM Timers, Power controls, External BUS Interface system Development and Debugging.

CASE STUDIES : Design of Embedded Systems using the micro controller – 8051/ARM6TDMI, for applications in the area of Communications, Automotives, industrial control.

SUGGESTED BOOKS

1. M.A. Mazadi & J.G. Mazidi, “The 8051 Micro Controller & embedded Systems”, Pearson Education. Asia (2002).
2. John B. Peatman, Designing with PIC Micro Controllers, Pearson Education
3. Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999.
4. Cathey May and Silha
5. (Ed)., “ The Power PC Architecture”, Morgan Kauffman Press (1998).

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I-Semester

ANALOG AND DIGITAL IC DESING

UNIT –I

OPERATIONAL AMPLIFIERS : General considerations one – state op-amps, two stage op-amps gais bcosting stage – comparison I/P range limitations slew rate. **CURRENT MIRRORS AND SINGLE STAGAE AMPLIFIERS:** simple CMOS, BJT current mirror, Cascode Wilson Wilder current mirrors. Common Source amplifier source follower, common gate amplifier

NOISE : Types of Noise – Thermal Noise – flicker noise – Noise in opamps – Noise in common source stage-noise band width.

UNIT – II

PHADED LOCKED LOOP DESIGN : PLL concepts – The phase locked loop in the locked condition Integrated circuit PLLs – phase Detector – voltage controlled oscillator – case study : Analysis of the 560 B Monolithic PLL.

SWITCHED CAPACITORS CIRCUIT : Basie Building blocks op-amps capacitors switches – non- over lapping clocks – Basic operations and analysis – resistor cquivalence of a switched capacitor parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis – First order filters- switch sharing fully differential filters – charged injections – switched capacitor – gain circuits parallel resistor – capacitor circuit – presettable gain circuit – other switched capacitor circuits – full wave rectifier peak detector – sinusoidal oscillator.

UNIT – III

LOGIC FAMILIES & CHARACTURISTICS : COMS, TTL, ECL, logic families CMOS,TTL, interfacing, comparison of logic families.

COMBINATIONAL LOGIC DESIGN USING VHDL: VHDL modeling for decoders, encoders, multipluxers, comparators, adders and subt actors.

SEQUENCIAL IC DESIGN USING VHD VHDL modeling for latches, flip flaps, counters, shift registers FSMs.

UNIT – IV

DIGITAL INTEGRADED SYSTEM BUILDING BLOCKS : Multiplexers and decoders – Barrel shifters counters digital single bit adder

MEMORIES : ROM : Internal structure 2D decoding commercial types timing and applications

CPLD : XC 9500 series family CPLD archi ecture, functional block internal architecture. I/O block internal structure.

FPGA: Conceptual of view of FPGA – classification based on CLB arrangement programming technologies – XC 4000 series family architecture – CLB internal architecture – I/O block architecture.

UNIT – V

COMPORATORS : Using an op-amp for a comparator – charge injection errors – latched comparator

NVQUIST RATE D/A CONVERTERS ; Decoder based converter resistor storing converters folded resister string converter – Binary scale converters – Binary weighted

resistor converters – Reduced resistance ratio ladders- R-2R based converters – Thermometer code current mode D/A converters.

NVQUIST RATE A/D CONVERTERS : Integrating coverters – successive approximation converters- DAC based successive approximation – flash converters time interleaved A/D Converters.

REFERENCES

1. Analog Integrated Circuit Design by David A.Johns, Ken Martin, John Willey & Sons.
2. Analysis and Design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley & Sons.
3. Design of Analog CMOS Integrated Circuits, Behzed Razavi. TMH
4. Digital Integrated Circuit Design by Ken Martin, Oxford University 2000
5. Digital Design Principles & Practices" by John F Wakerly, Pearson Education & Xilinx Design Series, 3rd Ed. (2002)

SUGGESTING READING

1. Ken martin, digital Integrated Circuit Design Ox ford University , 2000.
2. John F Wakerly, "Digital Design Principles & Practices", Pearson Education & Xilinx Design Series, 3rd Ed. (2002).
3. Samir Palnitkar, "Verilog HDL-A Guide to Digital Design and Synthesis", Prentice Hall India, (2002).
4. Douglas J Smith, "HDL Chip Design, a Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGA s using VHDL or Verilog, Doone Publications, (1999).

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I-Semester

EMBEDDED SYSTEMS CONCEPTS

UNIT –I
ANINTRODUCTION TO EMBEDDED SYSTEMS
An Embedded system, Processor in the system, other hardware units, software embedded into systems, exemplary embedded systems, embedded system on – chip (SOC) and in VLSI circuit Processor and memory organization – structural Units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded systems, allocation of memory to program cache and memory management links, segments and blocks and memory map of a system. DMA, interfacing processors, memories and Input Output Devices.

UNIT – II
DEVICES AND BUSES FOR DEVICE NETWORKS
I/O devices, timer and counting devices, serial communication using the "12C" CAN, profibus foundation field bus, and advanced I/O buses between the network multiple devices, host systems or computer parallel communication between the net worked I/O Multiple devices using the ISA, PCI, PCI-X and advanced buses.

UNIT – III
DEVIC DRIVERS AND INTERRUPTS SERVICING MECHANISM
Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt ser/ icing mechanism

UNIT –IV
PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C,C++, VC++ AND JAVA
Interprocess communication and synchronization of processes, task and threads, multiple processes in an application, problem of sharing data by multiple tasks and routines, interprocecss communication

UNIT-V
HARDWARE – Software co-design in an embedded system, embedded system project management, embedded system design and co-design issues in system development process, design cycle in the development phase for an embedded system, use of target systems, use of software tools for development of an embedded system, use of scopes and logic analysis for system, hardware tests. Issues in embedded system design.

TEXTBOOK
1. Embedded system: Architecture, programming and design by Rajkamal, TMH

REFERENCEs

1. Embedded system design by Arnold S Burger, CMP
2. An embedded software primer by David Simon, PEA
3. Embedded system design: Real world design be Steve Heath : Butterworth Heinenann. Newton mass USA 2002
4. Data Communication by Hayt .

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I-Semester

VHDL MODELLING OF DIGITAL SYSTEMS

UNIT –I
INTRODUCTION :
An Overview of Design Procedures Used for system design using CAD tools. Design entry, synthesis simulation, Optimization, place and route. Design Verification tools examples using commercial PC Based on VHDL elements of VHDL top down design with VHDL subprograms. Controller description VHDL Operators.

UNIT – II
BASIC CONCEPT IN VHDL :
Characterizing Hardware Languages, Objects and classes, signal Assignments, concurrent and sequential Assignments. Structural Specification of hardware : parts Library wiring of primitives, wiring interactive networks, modeling a test bench binding alternative op down wiring.

UNIT –III
DESIGN ORGANIZATIN AND PARAMETERIZATION :
Definition and usage if subprograms, packaging parts and utilities, design parametrization, design configuration, design libraries, utilities for high – level descriptions – type declaration and usage VHDL operators, subprogram parameter types and overloading, other types and type related Issues, predefined attributes, user defined attributes, packing basic utilities.

UNIT-IV
DATA FLOW DESCRIPTION IN VHDL
Multiplexing and data selection, state machine description, open collector gates, here state bussing a general data flow circuit, updating basic utilities behavioral description of hardware process statement assection statements, sequential wait statements formatted ASCII I/O operators, MSI – based Design .

UNIT – V
CPU MODELLING FOR DESCRIPTION IN VHDL :
Parwan CPU. Behavioural description of parawan, bussing structure, data flow deseription test bench for the parwan CPU. A more realistic parwan. Interface design and modeling VHDL as A modeling language.

TEXT BOOKS :
1. ZNAWABI : VHDL analysis and modeling of digital systems (2/E), megraw hill, (1998)

REFERENCE :
1. PERRY : VHDL, (3/E) mcgraw hill

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I-Semester

MODELING AND SYNTHESIS WITH VERILOG HDL (ELECTIVE –I)

UNIT –I

HARDWARE MODELING WITH THE VERILOG HDL :

Hardware encapsulation – the verilog module, hardware modeling verilog primitives, descriptive styles structural connections, behavioral description in verilog hierarchical descriptions of hardware, structured (top down design methodology, arrays of instances, using verilog for synthesis, language conventions, representation of numbers.

UNIT –II

LOGIC SSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL

User – defined primitives, user defined primitives – combinational behavior user – defined primitives sequential behavior, initialization of sequential primitives. Verilog variables, logic value set data types, strings. Constants, operators, expressions and operands operator precedence models of propagation delay; built- in constructs for delay signal transitions, veriolg models for gate propagation delay (Interila delay), time scales for simulation, verilog models for net delay (Transport delay) module paths and delays path delays and simulation inertial delay effects and pulse rejection.

UNIT – III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL :

Verilog behaviors, behavioral statements, procedural assignment, procedural continuous assignments, procedural timing controls and synchronization, intra-assignment, delay-blocked assignments, non-blocking assignment, intra-assignment delay : non- blocking assignment, simulation of simultaneous procedural assignments repeated intra assignment delay indeterminate assignments and ambiguity constructs for activity flow control, tasks and functions summary of delay constructs in verilog system tasks for timing checks variable scope revisited module contents behavioral models of finite state machines.

UNIT –IV

SYNTHESIS OF COMBINATIONAL LOGIC :

HDL – based synthesis, technology – independent design benefits of synthesis synthesis methodology vendor support, styles for synthesis of combinational logic technology mapping and shared resources, three state buffers, three state outputs and don't cares, synthesis of sequential logic synthesis of sequential udps, synthesis of latches synthesis of edge-triggered flip flops registered combinational logic shift registers and counters, synthesis of finite sate machines resets synthesis of gated clocks, design partitions and hierarchical structures.

UNIT –V

SYNTHESIS OF LANGUAGE CONSTRUCTS :

Synthesis of nets, synthesis of register variables, restrictions on synthesis of "X" and "Z" synthesis of expressions and operators, synthesis of assignments, 6 synthesis of case and conditional statement synthesis of resets, timings controls in synthesis, synthesis of multi-cycle operations, synthesis of loops, synthesis if fork join blocks, synthesis of the disable statement synthesis of user – defined tasks, synthesis of user – defined functions, synthesis of specify blocks, synthesis of compiler directives switch- level models in verilog MOS transistor technology, switch level models of MOS transistors switch level models of static CMOS circuits alternative loads and pull gates, CMOS transmission gates. Bio-directional gates (switches), signal strengths, signal strengths and wired logic. Design examples in verilog.

TEXTBOOK

1. M.D.CILETTI ; modeling synthesis and rapid prototyping with the verilog HDL (1999) PRENTICE – Hall .

REFERENCE

1. M.G.ARNOLD : verilog digital – computer design (1999) prentice – hall (ptr)

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I-Semester

HARDWARE- SOFTWARE CO- DESIGN
(ELECTIVE –I)

UNIT –I

CO- DESIGN ISSUES AND CO- SYNTHESIS ALGORITHMS :

Co- Design Models. Architectures, languages, a generic co-design methodology, hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

PROTOTYPING AND EMULATION AND TARGET ARCHITECTURES :

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure, target architectures and application system classes, architectures for control dominated system and data – dominated systems.

UNIT – III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES :

Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT – IV

DESIGN SPECIFICATION AND VERIFICATION :

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT – V

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN :

System – level specification, design representation for system level synthesis, system level specification languages, heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS :

1. Hardware / software co- design principles and practice, kluwer academic publishers

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I-Semester

LOW POWER VLSI DESIGN
(ELECTIVE –I)

UNIT –I

LOW POWER DESIGN, AN OVER VIEW : Introduction to low – voltage low power design, limitations, silicon-on-Insulator

UNIT – II

MOS/BiCMOS PROCESSES : Bi CMOS Processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT – III

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES : Deep subrnicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT – IV

DEVICE BEHAVIOR AND MODELING : Advanced MOSFET models, limitations of MOSFET models, Bipolar models.

UNIT – V

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybridmode environment.

UNIT –VI

CMOS AND Bi-CMOS LOGIC GATES : Conventional CMOS and BiCMOS logic gates. Performance evaluation

UNIT – VII

LOW-VOLTAGE LOW POWER LOGIC CIRCUITS : Comparison of advanced BiCMOS digital circuits ESD- free Bi CMOS, Digital circuit operation and comparative Evaluation.

UNIT – VIII

LOW POWER LATCHES AND FLIP FLOPS : Evolution of latches and flip flops-quality measures for latches and flip flops, Design perspective.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/Gohl(3authors)-Pearson Education Asia 1st Indian reprint,2002.

REFERENCES

1. Digital Integrated circuits, J.Rabaey PH.N.J 1996
2. CMOS Digital ICs sung-mokang and yusuf leblebici 3rd edition TMH 2003 (chapter 11)
3. VLSI DSP systems, parhi, john Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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I-Semester

R.F. MICROWAVE INTEGRATED CIRCUITS (ELECTIVE –II)

UNIT –I

Analysis and design of RF and microwave lines Review of transmission lines, parallel plate transmission line, low frequency solution, strip line and micro strip transmission lines, low frequency solution, high frequency properties of microslot line, co planer wave guides, coupled microstrip lines, spiral inductors capacitors.

UNIT –II

Microstrip/ stripline based filters. Resonators, phase shifters, micro strip based gyrators, circulators and isolators, directional couplers.

UNIT – III

Microwave active devices – microwave transistors, GaAs FETS (Structures, equivalent circuit). Low noise amplifiers, power amplifiers, oscillators, detectors, mixers, modulators and switches.

UNIT – IV

Technology of MICS: Deposition techniques vacuum evaporation vacuum sputtering ion plating MBE (Molecular Beam Epitaxy)- photo lithography, mask preparation, thick film technology, GaAs technology

UNIT – V

MIC Packaging : Component attachment bonding techniques, solder reflow techniques, input/output terminations, testing.

SUGGESTED BOOKS :

1. I kneppo and J. Fabian, “Microwave Integrated Circuit” , London : Chapman & hall (1994)
2. M.W. Medley, “Microwave and RF circuit: Analysis, Synthesis and Design” Artech House (1993).
3. R. Goyal, Monolithic Microwave Integraed Circuits: Technology & Design” Artech House (1998).
4. Y. Konishi, “ Microwave Integrated Circuit” Dekker, New York: Marcel Dekker, (1991)

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I-Semester

MICRO ELECTROMECHANICAL SYSTEMS (ELECTIVE –II)

UNIT –I

Introduction , basic structures of MEM devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMs) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatability of MEMS from the point of power dissipation, leakage tec.

UNIT –II

Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, distributed force, distributed force, deflection curves for canti levers- fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using laplace equation. Discussion on the approximate solutions – transient response of the MEMS.

UNIT – III

Two terminal MEMS - capacitance Vs voltage Curve – variable capacitor. Applications of variable capacitors. Two terminal MEM structures.
Three terminal MEM structures – controlled variable capacitors – MEM as a switch and possible applications.

UNIT – IV

MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR<simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping.
RF Switches for modulation.
MEM Transducers for pressure, force temperature. Optical MEMS.

UNIT – V

MEMTechnologies : silicon based MEMS- process flow – brief account of various processes and layers like fixed layer, moving layers spacers etc., etching technologies.
Metal Based MEMS : Thin and thick film technologies for MEMS. PROCESS flow and description of the processes. Status of MEMS in the current electronics scenario.

SUGGESTED BOOKS

1. GABRIEL. M. Review, R.F. MEMS theory, Design and Technology, John wiley & Sons, 2003.
2. Strength of Materials – by thimo shenko, CBS publishers & Distributors., 2000.
3. Ristic L. (Ed) sensor technology and Devices, Artech House, London 1994.
4. Servey E.Lyshevski, MEMS and NEMS, systems Devices; and structures, CRC press, 2002.

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II-Semester

EMBEDDED SOFTWARE DESIGN
(ELECTIVE –II)

UNIT –I

Pentium processor : introduction to the Pentium microprocessor, special Pentium registers, Pentium memory management .

UNIT –II

Embedded Design life ccle : introduction, product specification, hardware/software partitioning, iteration and implementation, detailed hardware and software design, Hardware/ software integration, product testing and release, maintaining and upgrading existing products selection process: packaging the silicon adequate performance, RTOS availability, tool chain availability, other issues in the selection process, partitioning decision: hardware/software duality, hardware trends, ASICs and revision costs.

UNIT – III

Development environment: The execution environment, memory organization system startup special Software techniques: manipulating the Hardware, interrupts and interrupt service routines (ISRs) watchdog times, flash memory design methodology. basic tool set: Host-Based debugging remote debuggers and debug kernels, ROM emulator, Logic analyzer.

UNIT – IV

BDM: Backgtound Debug mode, Joint Test Action Group (JTAG) and Nexus.
ICE- Integrated solution : Bullet proof Run Control, Real time trac, Hardware Break points, Overlay memory, timing constrains, usage issue, setting the trigger.
Testing : Why Test? When to Test? Which Test? When to Stop ? Choosing test cases, testing embedded Software performance testing maintenance and Testing, the future.

UNIT –V

Writing software for embedded systems: the compilation process, Native versus cross-Compilers, Runtime libraries, Writing a library, using alternative Libraries, using a standard Library, Proting kemels, extensions for embedded systems, Downloading. Emulation and debugging techniques: buffering and other data structures, What is a buffer? Linear Buffers, Directional Buffers, double buffering buffer exchange, linked list, FIFOs, circular buffers, buffer under run and overrun, allocating buffer memory memory leakage, memory and performance trade- offs .

TEXT BOOKS

1. Intel microporcessors by barry B Brey PHI
2. Embedded System Design – Introduction to Processes, Tools, Techniques, Arnold S Burger, CMP Books.
3. Embedded Systems Design by Steve Heath, newness.

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I-Semester

HDL PROGRAMMING AND EDA TOOLS LABORATORY

1. Digital Circuits Description using Verilog and VHDL
2. Verification of the functionality of designed circuits using function simulator
3. timing simulation for critical path time calculation
4. synthesis of digital circuits
5. Place and Route techniques for mojor FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital circuits using FPGA and CPLD devices

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II-Semester

VLSI TECHNOLOGY & DESIGN

UNIT –I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES : (MOS, CMOS, BiCMOS) Technology trends and projections.

UNIT- II

BASIC ELECTRICAL PROPERTIES OF MOS, COMS & BICOMS CIRCUITS: Ids-Vds relationships threshold voltage V_t, G_m, G_{ds} and W_o, pass Transistor, MOS, CMOS & Bi COMS Inverters, Zpu/Zpd, MOS transistor circuit model,latch-up in CMOS ircuits.

UNIT-III

LAYOUT DESIGN AND TOOLS : Transistor structures, Wires and Vias, Scalable Design rules layout Design tools.

UNIT – IV

LOGIC GATES & LAYOUTS: Static complementary gates switch logic, Alternative gate circuits low power gates, Resistive and Inductive interconnect delays.

UNIT –V

COMBINATIONAL LOGIC NETWORKS : Layouts, simulation, Network delay interconnect design power optimization, switch logic networks gate and network testing.

UNIT-VI

SEQUENTIAL SYSTEMS : Memory cell, and Arrays, clocking disciplines, Design power optimization design validation and testing.

UNIT-VII

FLOOR PLANNING & ARCHITECTURE DESIGN : Floor planning methods, off-chip connections, high level synthesis, Architecture for low power SOCs and embedded CPUs, Architecture testing.

UNIT-VIII

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout synthesis and Analysis, Scheduling and printing; Hardware/Software Co-design, chip design methodologies A simples Design example

TEXT BOOKS:

1. 1.Essentials of VLSI Circuits and Systems, K. Eshraghian et.al (3 authors PHI of India Ltd., 2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf, Pearrson Education, fifth Indian Reprint, 2005

REFERENCES :

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley.2nd edition
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990
3. CMOS Circuit Design Layout and simulation – Baker, Li Boyce, PHI,2004.

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II-Semester

REAL TIME OPERATING SYSTEMS FOR EMBEDDED SYSTEMS

UNIT –I

Introduction to Unix, overview of commands, file I/O, (open, create, close, Iseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Signals, Interprocess communication (pipes, fifos, message queues, semaphores, shared memory)

UNIT – II

Real Time systems: Typical real time application, Hard Vs soft real time systems, A reference model of Real Time Systems: Processors and resources, Temporal Parameters of Real Time workload, periodic task model precedence constraints and data dependency functional parameters, Resource parameters of jobs and parameters of resources. Commonly used approaches to Real Time Scheduling Clock driven, weighted Round Robin, Priority driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs online scheduling.

UNIT – III

Operating Systems : Overview, Time Services and Scheduling mechanisms, other basic operating systems function, processor reserves and resource kernel. Capabilities of commercial Real Time Operating Systems.

UNIT- IV

Fault Tolerance Techniques : Introduction, Fault causes, Types, Detection, Fault and error containment, Redundancy : Hardware, Software, Time. Integrated Failure handling.

UNIT – V

Case Studies : VX works: Memory managements task state transiton diagram, per- emptive prioriy, scheduling context switches – semaphore – Binary mutex, counting watch dugs, I/O system RT Lintix : Process Management, Scheduling, Interrupt management, and synchronization

TEXT BOOKS

1. Advanced Unix Programming Richard Stevens
2. Real Time Systems – Jane W.S.Liu – Pearson Education
3. Real Time systems – C.M.Krishna, KANG G.Shin – M.G.Hill
4. Vx Works Programmers Guids

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II-Semester

DSP PROCESSORS AND ARCHITECTURES

UNIT –I
INTRODUCTION TO DIGITAL SIGNAL PROCESING
Introduction, A Digital signal-Processing system, The sampling process, Discrete time sequences. Discrete fourier transform (DFT) and fast fourier transform (FFT) Linear time-invariant systems, Digital filters Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB

UNIT –II
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS
Naumber formats for signals and coefficient in DSPsystems, Dynamic range and precision source of error in DSP implementations,A/D Conversion errors, DSP Computational errors, D/A Conversion Errors Compensating filter.

UNIT-III
ARCHITECTURES FOR PROGRAMMABLE DSPDEVICES
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and memory data addressing capabilitics, address generation unit,programmability and program execution speed Issues features for external interfacing.

UNIT -IV
EXECUTION CONTROL AND PIPELINING
Hardware looping, interrupts, Stacks, relative branch support pipelining and performance, pipelir,e depth interlocking branching effects. Interrupt effects, pipeline programming models.

UNIT – V
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS
Commercial Digital signal-processing devices, data addressing modes of TMS320C54XX DSPs. Data addressing modes of TMS320 C54XX Processors. Memory space of TMS 320C54XXX Processors, Program control. TMS 320C54XX instructions and Programming, On-chip Peripherals, interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors.

UNIT –IV
IMPLEMENTATIONS OF BASIC DSP ALGORITMS
The Q- notation, FIR filters, IIR filters, It terpolation filters, Decimation filters, PID controller, Adaptive Filters, 2-D Signal Processing.

UNIT – VII
IMPLEMENTATION OF FFT ALGOR THMS
An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-point FFT implementation on the TMS 320C54XX, Computation of the signal spectrum.

UNIT – VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, external bus interfacing signals, Memory interface, parallel i/o interface programmed I/O, Direct memory access (DMA)

A Multicihannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. digital signal processing Avtar singh and S.Srinivasan, Thomson publications,2004
2. DSP Processor Fundamentals Architectures & features – lapsley et al, S. Chand & Co,2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications –B. Venkata Ramani and M. Bhaskar, TMH, 2004
2. Digital signal processing – Jonathan Stein, john Wiley-2005

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II-Semester

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

UNIT –I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice pLST's architectures – 3000 series – Speed performance and in system programmability.

UNIT – II

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT – III

Finite state machines (FSM) top down design state transition table, state assignments for FPGAs problem of initial state assignment for one hot encoding. Derivations of state machine charges, realization of state machine charts with a PAL. Alternative realization for state machine chat suing microprogramming linked state machine one –hot state machine, petrinetes for state machines-basic concepts, properties, extended petrinetes for parallel controllers.

UNIT – IV

FSM Architectures and systems level design: architectures centered around non-registered PLDs state machine designs centered around shift registers. One – Hot design method. Use of ASMs in One-Hot design. K application of One-Hot method. System level design- controller, data path and functional partition.

UNIT-V

Digital front end digital design tools for FPOGAs& ASICs: Using mentor graphics EDA tool ("FPGA Advantage") – Design flow using FPGAs – Guidelines and Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, parellel controllers.

SUGGESTED BOOKS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate array, jprentice Hall (Pre). 1994.
2. S. Trimberger, Edr., Field Programmable gate array technology Kluwer academic publicatgions. 1994.
3. j. old field, R.Dorf, fieldprogramnable gate arrays, john wiley &sons,Newyork, 1995.
4. S. Brown, R.Francis, J.Rose ,Z.Vransic, Field programmable gate array, kluwer pubin, 1992.

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I-Semester

DESIGN FOR TEST ABILITY
(ELECTIVE –III)

UNIT –I

Introduction to test and design for testability (DFT) fundamentals.

Modeling: Modeling digital circuits at logic level, register level and structural models. Levels or modeling

Logic simulation: Types of simulation, Delay models, Element evaluation, hazard detection, gate level event driven simulation.

UNIT – II

Fault modeling – Logic fault models, fault detection and redundancy, fault equivalence and fault models. Vector simulation ATPG vectors, formats, compaction and compression, selecting ATPG Tool.

UNIT – III

Testing for single stuck faults (SSF) Automated test pattern generation (ATPG/ATG) FOR SSFs in combinational and sequential circuits, functional testing with specific fault models. Vector simulation ATPG vectors, formats, compaction and compression, selecting ATPG Tool.

UNIT – IV

Design for testability – testability trade- offs, techniques, Scan architectures and testing controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design board level and system level DFT approaches. Boundary scans standards, compression techniques different techniques. Syndrome test and signature analysis.

UNIT- V

Built-in self-test (BIST) – BIST concepts and tst pattern generation. Specific BIST ARCHITECTURES – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, PILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST): Memory test architectures and techniques- Introduction to memory test types of memories and integration, Embedded memory testing model, Memory test requirements for MBIST Brief ideas on embedded core testing.

Introduction to automatic in circuit testing (ICT), JTAG Testing features.

SUGGESTING READING

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico publishing House, 2001
2. Alfred Crouch, Design for test for Digital ICs & Embedded Core systems, prentice Hail
3. Robert J.Feugate, Jr.Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall Englehood Cliffs, 1998.

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II-Semester

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE – III)

UNIT –I

PRELIMINARIES :

Introduction to Design Methodologies, Design Automation tools, Algorithimic Graph theory, Computational complexity, tractable and intractable problems.

UNIT –II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION : Backtracking branch and bound, Dynamic programming Integer linear programming local scarch simulated annealing tabu search Genetic Algorithms.

UNIT –III

Layout compaction, placement, Floorplanning and routing problems, Concepts and algorithms

UNIT –IV

MODELLING AND SIMULATION : Gate level modeling and simulation switch level modeling and simulation.

UNIT –V

LOGIC SYNTHESIS AND VERIFICATION : Basic issues and terminology binary decision diagrams two-level logic synthesis

UNIT – VI

HIGH-LEVEL SYNTHESIS : Hardware Models, internal representation of the input algorithm, allocation assignment and scheduling, some scheduling algorithms, some suspects of assignment problem, high level transformations.

UNIT – VII

PHYSICAL DESIGN AUTOMATION OF FPGA'S FPGA technologies, physical design cycle for FPGA's, partitioning and routing for segmented and staggered models.

UNIT – VIII

PHYSICAL DESIGN AUTOMATION OF MCM'S MCM technologies, MCM physical design cycle, partitioning, placement – chip array based and full custom Approaches, Routing- Maze routing multiple stage routing. Topologic routing integrated pin – distribution and routing, routing and programmable MCM's .

TEXTBOOKS :

1. Algorithms for VLSI Design automation, S.H. Gerez, WILEY student edution, john wiley & sons (Asia) pvt. Ltd., 1999.
2. Algorithms for VLSI physical Design automation, 3rd edution, Naveed sherwani, sqringer international edition, 2005.

REFERENCES

1. Computer aided logical Design with emphasis on VLSI-Hill & Peterson, wiley, 1993
2. Modern VLSI Design: systems on silicon – Wayne Wolf, Pearson education Asia, 2nd Editior, 1998

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II-Semester

NETWORK SECURITY AND CRYPTOGRAPHY
(ELECTIVE – III)

UNIT –I

INTRODUCTION : Attacks, services and Mechanisms, Security attacks, Security services. A Model for internetwork security .

CLASSICAL TECHNIQUES : Conventional Encryption model, Steganography, Classical Eneryption Techniques.

UNIT – II

MODERN TECHNIQUES : Symplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

ALGORITHMS : Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST- 128, RC2 Characteristics of Advanced symmetric block cifers.

UNIT – III

CONVENTIONAL ENCRYPTION : Placement of encryption function, Traffic confidentiality, key distribution, Random Number Generation.

PUBLIC KEY CRYPTOGRAPHY : Principles, RSA Algorithm, Key Management. Diffie-Hellman key exchange, Elliptic Curve Cryptograpy.

UNIT – IV

NUMBER THEORY : Prime and relatively prime numbers, modular arithmetic. Fermat's and euler's theorems, Testing for primality, euclid's Algorithm, the Chinese remainder theorem, discrete logarithms.

MESSAGE AUTHENTICATION AND HASH FUNCTIONS : Authentication requirements and functions. Message authentication, Hash functions, Security of Hash functions and MACs.

UNIT – V

HASH AND MAC ALGORITHMS : MD file, Message digest algorithm, Secure Hash algorithm RIPEMD – 160, HMAC.

DIGITAL SIGNATURES AND AUTHEMTICATION PROTOCOLS : Digital signatures. Authentication protocols, digital signature standards.

UNIT – VI

AUTHENTICATION APPLICATIONS : Kerberos, X, 509 directory authentication service.

ELECTRONIC MAIL SECURITY : PRETTY GOOD PRIVACY, S/MIME.

UNIT – VII

IP SECURITY : Overview, Architecture, authentication encapsulating security payload. Combining security associations, Key management.

WEB SECURITY : Web security requirements, Secure sockets layer and Transport layer security secure electronic transaction.

UNIT – VIII

INTRUDERS, VIRUSES AND WORMS : Intruders, Viruses and Related treats,
Fire Walls : Fire wall Desing principles, Trusted Systems.

TEXT BOOKS

1. Cryptography and Net work security : Principles and Practice – William stallings, Pearson Education .,2000.

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II-Semester

IMAGE AND VIDEO PROCESSING
(ELECTIVE – IV)

UNIT – I

Fundamentals steps of Image Processing, Components of an Image processing system, Image sampling and quantization, relationship between the pixels. Gray level transformation, Histogram processing, Smoothing and sharpening spatial filters, Smoothing and sharpening frequency domain filters, Homomorphic filtering Restoration filters – spatial and frequency domain, Inverse filter, Wiener filter

Color image processing: Pseudo color image processing, Color transformation, Smoothing and sharpening

UNIT – II

Morphological operations: Dilation and erosion, Opening and closing, Hit or Miss transforms, Morphological algorithms, Extensions to gray scales images and its applications.

Image compression: Compression models, Error free coding, lossy coding, compression standards, color image compression.

Image segmentation: Edge linking and boundary detection, Thresholding, Region based segmentation. Segmentation by morphological watersheds, color segmentation

UNIT – III

Video formation, perception and representation: Color perception and specification, Video capture and display, Analog video raster, Analog color TV systems, Digital Video

Video Sampling: Basics of lattice theory, sampling over lattice, Sampling of video signals, filtering operations, Conversion of signals sampled on different lattice, Sampling rate conversion of video signals.

UNIT – IV

Video modeling: Camera model, illumination model, object model. Scene model, Two dimensional motion models

2 –D motion estimation: Optical flow, General methodologies, Pixel based motion estimation, Block matching algorithm, Mesh – based motion estimation, Global motion estimation, Region based motion estimation, Multiresolution motion estimation. Application of motion estimation in video coding

UNIT – V

Video coding: Information theory, Binary encoding, Scalar quantization, Vector quantization, Waveform based video coding: Block based transform coding, Predictive coding, Object based scalability, Wavelet Transform based coding.

REFERENCE BOOKS

1. Digital Image Processing – Gonzaleze and woods
2. Video processing and communication – Yao Wang, Joern Ostermann and Ya – Qin Zhang. Prentied Hall
3. Digital video processing – M.Tekalp

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II-Semester

SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION
(ELECTIVE – IV)

UNIT -1
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

UNIT -II
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied variables.

UNIT -III
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT -IV
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL.

UNIT -V
Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

SUGGESTED READING:

1. Randal L; Schwartz Tom Phoenix, "Learning PERL", Orcilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, "Programming PERL" , Orcilly Publications, 3rd Edn., 2000.
3. Tom Christiansen, Nathan Torkington, PERL Cookbook, Orcilly Publications, 3rd Edn, 2000.

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II – Semester

ADVANCED DIGITAL FILTERING
(ELECTIVE – IV)

UNIT – I

Multirate Digital Signal Processing: Introduction – Decimation by integer factor, interpolation by an integer factor. Sampling rate conversion by non – integer factors, Multistage approach to sampling rate conversion. Design of practical sampling – rate converters. Software implementation of interpolators and decimators. Sample rate conversion using polyphase filter structure. Examples of applications of multirate DSP.

UNIT – II

Linear prediction and optimum linear filters: Representation of a stationary random process. Rational power spectra – A.R. M.A & ARMA processes. Relationship between the filter parameters and Auto-correlation sequence. Forward and Backward linear prediction. Optimum reflection coefficient for the Lattiee forward and backward and backward predictors. A.R. process and linear prediction Solution of Normal equations. Levinson-Durbin algorithm. The schur algorithm. Pipelined architecture for implementing the Schur algorithm. Properties of linear Prediction error filters. AR Lattice and ARMA Lattiee – Ladder filters.

UNIT – III

Adaptive Digital filters: Concepts, Basic wiener filter theory, Basic LMS adaptive algorithm, Recursive least squares algorithm, Application examples.

UNIT -IV

Applications of Adaptive filters: Adaptive channel equalization, Echo cancellation in Data Transmission over Telephone channels, Adaptive noise canceling.

UNIT -V

Recursive Least Squares Algorithms for array signal processing: QR Decomposition for least squares Estimation, Estimation of spectra from finite. Duration observation of signals: Parametric and non parametric methods for power spectrum Estimation

REFERENCES

1. E.C. Ifeachor et.al., Digital Signal Processing, Pearson Education
2. John G.Proakis, C.M.Radar, Algonthms for statistical signal processing Pearson Education.
3. Dimitirs G.Manolakis Statistical & Adaptive Signal Processing TMH.

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II – Semester

EMBEDDED SYSTEMS DESIGN LAB
(ELECTIVE – IV)

1. Study of Real Time Operating Systems.
2. Development of Device Drivers for RT Linux.
3. Software Development for DSP Applications.
4. Serial Communication Driver for ARM Processors.
5. LCD Interface using 8051 Microcontroller.
6. Keyboard / Display Interface using M68HC11 controller.
7. Implementation of Timer/ Counter using PIC Microcontroller.
8. Case Study:
   (a) Microcontroller Design Tools.
   (b) Design of RTOS Kernel.
   (c) Cross compiler / Assembler.
   (d) Vx Works.