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ACCREDITED BY NAAC
A-GRADE

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

(Established by Govt. Act No. 30 of 2008)

Kukatpally, Hyderabad – 500085, Telangana, India

Dr. M. Manzoor Hussain
M.Tech., Ph.D.,
Professor of Mechanical Engineering &
REGISTRAR

Lr. No. JNTUH/DAAF/A3/2499/2023 Date.05.07.2023

To
The Director,
VEDA Educational Society,
2nd Floor, Aydiv IT Park,
Puppalaguda Village, Rangareddy District.

Sir,

Sub: JNT University Hyderabad – DAAF – To approve the proposal for Integrated Dual Degree program in two disciplines in VLSI Engineering and Embedded System Design with a facility to transfer credits earned at VEDA IIT - Reg.

Ref: 1. The MOU was extended on 16.06.2022.
2. Letter dated. 21.04.2023 of the Director, VEDA IIT, Hyderabad.
3. 58th meeting Standing Committee of the Academic Senate held on 23.05.2023.
4. Letter dated. 21.06.2023 of the Director, VEDA IIT, Hyderabad.
5. Note orders of the Vice-Chancellor dated. 24.06.2023.

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With reference to the letter (1) cited, the Director, VEDA IIT has proposed "Integrated Dual Degree Programs (IDP)" for 3rd year-completed students of JNTUH (University, Autonomous and Affiliated Colleges) in two disciplines (i) VLSI Engineering and (ii) Embedded System Design leading to B.Tech. & M. Tech. degrees through specialized training in the Industry eco-system to cater to the academics of the 4th year of B.Tech. and an additional 5th year.

Hence, the Director, VEDA IIT has requested the University to approve the proposal for Integrated Dual Degree Program in two disciplines in VLSI Engineering and Embedded System Design with a facility to transfer credits earned at VEDA IIT.

In the reference (4) cited above, the Director, VEDA IIT has submitted modified course structure and credits requirements (as per R18 regulations of JNTUH IDP program) for Integrated Dual Degree program in two disciplines in VLSI Engineering and Embedded System Design with a facility to transfer credits earned at VEDA IIT. The revised course structure is as follows:

IV Year I Semester:

S. No.	Group	Course Title	Marks					
			Int.	Ext.	L	T	P	C
1	PC (UG)	Advanced Logic Design with Functional Blocks & State Machines	30	70	3	1	0	4
2	PC (PG)	VLSI Design with Verilog	30	70	4	0	0	4
		X86 Architecture						
3	PE-III (UG)	VLSI Analog Design	30	70	3	0	0	3
		C++ & Verification Methodologies						
		VLSI Physical Design Essentials						
		C++ & Date Structures in C						
4	OE-II (UG)	Unix, PERL & TCL	30	70	3	0	0	3
		Unix, Python & TCL						
5	PCL (PG)	VLSI Verilog Design & Verification Lab	30	70	0	0	6	3
		X86 Lab						

6	PEL (UG)	VLSI Analog Design Lab	30	70	0	0	4	2
		C++ & Verification Methodologies Lab						
		VLSI Physical Design Essentials Lab						
		C++ & Data Structure in C Lab						
7	OEL (UG)	Unix, PERL & TCL Lab	30	70	0	0	4	2
		Unix, Python & TCL Lab						
8	PC (UG)	Project Stage-I	30	70	0	0	6	3
		Total	**240**	**560**	**13**	**1**	**20**	**24**

IV Year II Semester:

S. No.	Group	Course Title	Marks					
			Int.	Ext.	L	T	P	C
1	PC (PG)	VLSI Synthesis	30	70	4	0	0	4
		Advanced Processor Architecture						
2	PE-IV (UG)	Analog Mixed Signal Design	30	70	3	0	0	3
		System Verilog Assertions & UVM						
		VLSI Advanced Physical Design						
		Real-Time Operating Systems						
		Introduction to Web Development						
3	OE-III (PG)	High- Speed CMOS Design	30	70	4	0	0	4
		Design for Testability-Logic Design						
		Design for Testability – Physical Design						
		DSPs & Architectures						
		Full Stack						
		Core JAVA						
4	PC (UG)	Project Stage-II, including report & Viva-Voce	30	70	0	0	20	10
		Total	**120**	**280**	**11**	**0**	**20**	**21**

V Year I Semester:

S. No.	Group	Course Title	Marks					
			Int.	Ext.	L	T	P	C
1	PG	Dissertation Phase-I	30	70	-	-	48	24
		Total:	**30**	**70**	-	-	**48**	**24**

V Year II Semester:

S. No.	Group	Course Title	Marks					
			Int.	Ext.	L	T	P	C
1	PG	Dissertation Phase-II	30	70	-	-	42	21
2	PG	Project Evaluation (Viva -Voice)	0	100	-	-		4
		Total	**30**	**170**				**25**

As per note orders of the higher authorities, the proposal was placed in the 58th meeting of the Standing Committee of Academic Committee. The Standing Committee resolved to approve the proposal for Integrated Dual Degree program in two disciplines in VLSI Engineering and Embedded System Design with a facility to transfer credits earned at VEDA IIT in Industry eco-system to JNTUH for the award of B.Tech & M.Tech degree for B.Tech students of JNTUH (University, Autonomous and Affiliated Colleges) who completed 3rd year (Regular/Full Time).

Based on the recommendations of the Standing Committee of the Academic Senate, the Hon'ble Vice-Chancellor is pleased to approve the proposal for Integrated Dual Degree program in two disciplines in VLSI Engineering and Embedded System Design with a facility to transfer credits earned at VEDA IIT in Industry eco-system to JNTUH for the award of B.Tech & M.Tech degree for B.Tech students of JNTUH (University, Autonomous and Affiliated Colleges) who completed 3rd year (Regular/Full Time).

Yours sincerely,

05/7/23

REGISTRAR

Encl: Admission procedure.

Copy to:
The Principals of the all JNTUH University Engineering Colleges,
The Principals of the all Autonomous and Affiliated Engineering Colleges of JNTUH.
The Directorate of University Examinations (DUEX), JNTUH
The Controller of Examinations, JNTUH.
PA to VC/Rector/Registrar for information…

GATEWAY TO A LUCRATIVE CAREER IN SEMICONDUCTOR INDUSTRY

VEDA IIT OFFERS

VEDA
Learn. Explore. Excel.

INTEGRATED DUAL DEGREE PROGRAMS (IDP)

VLSI ENGINEERING
EMBEDDED SYSTEM DESIGN

(JNTUH approved & Consortium sponsored)

Leading to a prospective job in consortium/associated companies

with a facility to transfer credits earned at VEDA IIT to JNTUH for the award of B.Tech & M.Tech degrees

for B.Tech students who completed 3rd year in JNTUH Constituent, Affiliated and Autonomous Colleges

in collaboration with

SoCtronics & invecas

VEDA IIT, one of the top VLSI Engineering Institutes, conducts the program

Knowledge-intensive and Industry-Oriented Program

JNTUH approved credits transfer for 4th year of B.Tech and additional 5th year for M.Tech

Internship with Stipend in 5th year and subsequent employment in consortium company*

*Terms and conditions apply. For details contact HR, VEDA IIT

COMMON ENTRANCE TEST

Preliminary Test: 23rd July, 2023; 9:30 AM - 10:30 AM

Main Test: 23rd July, 2023; 2:00 PM - 4:00 PM

Test Center for Preliminary & Main: VEDA IIT, Hyderabad

Last Date to apply: 22nd July, 2023; 1:00 PM

Syllabus: visit www.vedaiit.org/idp

Apply online at www.vedaiit.org

ELIGIBILITY & ADMISSION

- **Students of JNTUH Constituent, Autonomous & Affiliated colleges, completing B.Tech. III year by 24th July, 2023 in ECE/EEE/EIE/CSE**
- **Those who have taken our main test on 4th June 2023 can apply but need not take the test again, as their performance in that test will be considered for the selection**
- **Admission: Based on performance in the entrance tests & interview**
- **Program is likely to commence from 25th July, 2023**

ABOUT VEDA IIT

- **Expert faculty from reputed VLSI Design Houses/Institutes**
- **Industry projects with proven design methodologies at cutting edge technologies**
- **Well-equipped infrastructure with high-end state-of-the-art computing facilities**
- **Excellent placement track record in leading Technology Companies since inception**
- **Partnership with global leaders of technology**
- **Innovative Teaching-Company model with Industry and University participation - first of its kind**
- **Listed among top five institutes in VLSI Engineering by Times of India**
- **Pioneered in incubating many successful design teams/companies**
- **Lead organizers of International VLSI Conferences - VLSI 2006, 2008, 2012 & 2017**
- **Holistic education covering various aspects of VLSI and System Design**

Hands-on Experience with best-in-class tools covering the entire ASIC design flow from the world class EDA Vendors

cadence™ Mentor Graphics SYNOPSYS® Silicon to Software

VEDA
Learn. Explore. Excel.

VEDA IIT, A Unit of The VEDA Educational Society

Regd. No. 410/2014 | hr@vedaiit.org

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