GATEWAY TO A LUCRATIVE CAREER IN SEMICONDUCTOR INDUSTRY

Learn. Explore. Excel.

Engineer Trainee Recruitment in

VLSI DESIGN/EMBEDDED SYSTEM DESIGN

Industry-Ready Professional Training
leading to a job in associated companies including MNCs

(Company sponsored & JNTUH approved)

In fulfilment of coursework for 2 Semesters of B.Tech 4th Year
JNTUH Constituent, Affiliated and Autonomous Colleges

in collaboration with

SoCtronics & invecas

VEDA IIT, one of the top VLSI Engineering Institutes, conducts the program

Knowledge-intensive and Industry-Oriented Program

JNTUH approved transfer of 40 credits earned at VEDA IIT for award of B.Tech Degree

Internship with Stipend in 2nd Sem. and subsequent employment in consortium company*

*Terms and conditions apply. For details contact HR, VEDA IIT

COMMON ENTRANCE TEST

Preliminary Test(Online): 3rd Aug, 2022; 10 AM - 11 AM
Main Test(Offline): 6th Aug, 2022; 10 AM – 1 PM
Test Center: Hyderabad
Last Date to apply: 31st July, 2022
Syllabus: visit www.vedaiit.org

Apply online at www.vedaiit.org

ELIGIBILITY & ADMISSION

- **Students of JNTUH Constituent, Autonomous & Affiliated colleges, completing B.Tech. III year by 23rd Aug, 2022 in ECE/EEE/EIE/CSE & other allied branches**
  (Ref: JNTUH Circular dt. 20th July, 2022 at http://jntuh.ac.in)
- **Admission: Based on performance in the entrance tests & Interview**

About VEDA

- Expert faculty from reputed VLSI & Embedded System Design Companies/ Institutes
- Well-equipped Labs with high-end, state-of-the-art computingfacilities
- VEDA trained engineers are equipped with the required skills to work on state-of-the-art technology solutions, collaborating with global technology teams
- Innovative Teaching Company with Industry and University participation - First of its kind. Pioneered in incubating many successful design teams/ companies
- One of the top five institutes in VLSI Engineering as ranked by Times of India
- Received laurels as the best industry-oriented training institute in VLSI and Embedded System design from global design companies

About SoCtronics

- Customer-focused VLSI and Embedded system design services company
- Offers spec-to-system turnkey solutions involving all aspects of chip design and embedded software
- Proven design methodologies enabling first-time silicon success for many complex ASICs; Partner of technology start-ups for their new and innovative product solutions
- Key industries: Computing, Graphics, Automotive, IoT, Consumer Electronics, Medical, Defense, Mobile
- Work on cutting edge technology nodes below 7nm, Turnkey silicon solutions for AI/ML, Automotive and Networking markets, and Embedded software solutions for multimedia, network protocols, application frameworks and stacks
- Work with top-tier semiconductor and system companies across the world

Hands-on Experience with best-in-class tools covering the entire ASIC design flow from the world class EDA Vendors

cadence™ Mentor Graphics SYNOPSYS® Silicon to Software™

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VEDA IIT, A Unit of The VEDA Educational Society
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Andhra Pradesh: Vidyanagar, 1st Lane & 1st Cross, Guntur 522 007
HYD: 040 - 43929999 | +91 9989928276 | GNT: 0863 - 2374000 | +91 8328535061

Engineer Trainee Recruitment in VLSI Design/Embedded System Design
Industry Ready Professional Training
For B.Tech. ECE/EEE/EIE/CSE 4th Year I & II Semesters (JNTUH Approved)

Sponsored training leading to a job at SoCtronics/Associated Companies

Coordinated and Conducted by JNTUH & VEDA IIT

Job Requirement Form(JRF) for the drive on August 03, 2022

Company Name(s):	SoCtronics Technologies Pvt Ltd www.soctronics.com, Or any other associated companies having MoU with VEDA IIT for recruitment and sponsored training
Address:	**VEDA IIT** Telangana: 2nd Floor, AYDIV IT Park, Puppalaguda, Rangareddy 500 032 Andhra Pradesh: Vidyanagar, 1st Lane & 1st Cross, Guntur 522 007
Eligibility	B.Tech. Students of JNTUH completing 3rd year by 23rd Aug 2022 in Electronics/ Electrical/ Computer Science/ Instrumentation and allied branches with a minimum 70% marks or equivalent at all stages.
Salary Package:	**SoCtronics:** **VLSI Design**: ₹6 to 9 Lakhs for Engineer Trainee in 1st year after successful completion of sponsored training at VEDA IIT and based on performance in the training **Embedded System Design**: ₹5 to 6.5 Lakhs for Engineer Trainee in 1st year after successful completion of sponsored training at VEDA IIT and based on performance in the training **Other associated companies:** On successful completion of B.Tech. and sponsored training at VEDA IIT and based on performance in the training, VEDA IIT will facilitate employment offers from other associated companies including MNCs as per their selection, requirements and terms & conditions of employment
Job Location:	For SoCtronics : Hyderabad/Guntur For other associated companies: Their respective locations
Terms & Conditions :	Selected B.Tech IV year I semester students will be offered sponsored training, internship, and subsequent employment by SoCtronics, as per the following terms & conditions. **SoCtronics:** In consideration of the training cost involved and the sponsorship offered, the selected candidate shall agree to continue his/her employment for a minimum period of 3 years after joining as an Engineer Trainee on the terms and conditions made known to the candidates. In the event of discontinuance of training and employment, the candidate shall compensate the company for the training cost (Training cost reimbursement cost) in a pro-rated manner as set out below: • ₹ 8 lakhs if training has not been completed/discontinued or employment is discontinued prior to completion of 1 yr. from the date of joining the employment. However, for candidates leaving for higher studies in Premier foreign Universities/IITs or for an Indian Government job of Group 1 and above, during the 4th year or after completion of B. Tech. but before joining the employment, in addition to any payment received by them, 50% of the Training cost reimbursement amount (subsidized by the company) is to be paid by them considering them as special cases on submission of evidence of joining • ₹ 6 lakhs if employment is discontinued prior to completion of 2nd year from the date of joining the employment. • ₹ 4 lakhs if employment is discontinued prior to completion of 3rd yr. from the date of joining the employment. • Training cost reimbursement requirement is fully waived after 3 years of employment in the Company. • In the case of Embedded System Design the compensation is reduced by 1 lakh
Note: Terms and conditions of other associated companies will be communicated at the time of their final selection after successful completion of training	

Job titles and Job Description: Engineer Trainee in the 1st year and Engineer-1 in the 2nd year for SoCtronics.

VLSI Logic Design (RTL): Logic design entails working with a high-level architecture specification of the product and coming up with the micro-architecture specification, converting the micro-architecture specification into efficient Verilog RTL code, at IP or SOC level. Designers need to work at the SoC level to integrate the various IP blocks and tune the architecture to meet the performance requirements of the product and also closely work with DV engineers to help fix the bugs and solve any issues that arise during the design cycle.

VLSI Digital Verification: Digital Verification domain deals with verifying the correctness of the functionality of a given design against its specification. Verification Cycle mainly includes Test Plan, Test Stimulus, Test bench, Coverage development, DV Metrics Closure, and DV Signoff. It is performed at various levels like IP, Subsystem, SOC, and Multi-Chip SOC. RTL or Gate level Simulation, Emulation, and Formal Verification are some of the techniques involved in DV.

VLSI Physical Design (PD): Physical design is a process of converting logical connectivity of cells (netlist) into physical connectivity (manufacturable layout) meeting power, performance, and area requirements. All design components are instantiated with their geometric shapes and have appropriate routing connections in metal layers. This involves Physical Placement & Routing, Functional Equivalence, Timing Closure, Verification of correct electrical and logical functionality of physical design vs logic design, manufacturability, and yield using EDA tools before the design is taped-out for semiconductor fabrication.

VLSI Design Implementation: Design implementation involves the conversion of high-level design intent specified in RTL to logical gates known as synthesis, and the development of timing constraints to help Physical design engineers close the timing/performance targets. The implementation also entails the insertion of Design For Test (DFT) structures to help test the design post-fabrication for any manufacturing defects. Complex submicron designs with billions of logic gates and multiple MB of memory are tested using DFT in a fraction of the time compared to exhaustive functional verification tests.

Embedded Software Development (ESW): Engineer is responsible for the design and development of embedded software consisting of device drivers, Algorithms implementation of the DSP and RISC processors, understanding the RTOS concepts and developing the functions meeting the real-time constraints. This domain requires an understanding of CISC/RISC processor and Microcontroller architectural features, the functionality of standard peripheral controllers, and equipped with proficient programming skills in C and Assembly languages, and RTOS.

Application Software Development (ASD): The application Software Developer is responsible for developing, different kinds of applications that must run on embedded devices/systems like Mobile phones, Set Top Box, Smart TV, and Smart Watch, either directly or a companion device or on the web and also standalone applications which run on desktop/ laptops that may pair up with the embedded devices and systems for configuration and control. This domain requires skills for relational and non-relational databases, frontend user interface and backend logic, understanding of the product (mobile / TV / Web) and the end users.

Software QA and Automation (SWT): The software QA engineer is responsible to verify and certify that the software that is being released is of high quality and has been thoroughly tested. The software QA engineers need to understand the product requirements and functionality deeply and automate the testing by either using existing automation frameworks or developing brand-new automation frameworks using any of the scripting languages like Python, Ruby, etc. The work also involves developing continuous integration pipelines and doing release management and sign-off.