Jawaharlal Nehru Technological University, the **First Technological University** of India, was established on 2nd October 1972 in Andhra Pradesh with head quarters located in **Hyderabad.** The University is one of the premier Universities in India, accredited by **NAAC** with **'A'** Grade. After successful and proven levels of appreciated existence and stature spanning over 36 years, JNTU has been divided into four different Universities by Govt. of Andhra Pradesh, through Act No.30, Dt. 24th September, 2008. JNTU Hyderabad is one among the four Universities. Its Constituent college, "JNTUH College of Engineering, Hyderabad" is regarded as a pioneer in Technical Education and is a flagship College of the University. Other constituent colleges of JNTUH are located at Jagityal, Sultanpur, Manthani and other academic units at Hyderabad campus.

Directorate of University Industry Interaction Center (D-UIIC)

JNTU Hyderabad has been a pioneer in promoting industry-academia interaction and the scope of the activities has been steadily growing. In this endeavour, JNTUH has established a Directorate of University Industry Interaction Centre (UIIC) in the year, 2009. Industry interactions relating to Engineering and Technology, Basic and Applied Sciences, Pharmacy and Management come under the umbrella of University Industry Interaction Centre. The main focus of UIIC is to bridge the gap between Industry requirements and Academic delivery. The UIIC carries forward the interaction of University with the industrial bodies of Public, Private and Government sector organizations.

Functions/ Activities of UIIC

- Industry Collaborative Activities to the Students & Faculty
- Career Guidance & Training to the Students
- Placements to the Students

Objectives of UIIC

- UIIC helps the Industry to hire the right talent from its students' community at the right time.
- UIIC facilitates the students' internships, academic projects, training programs and Placements for the Students by the Industries.
- Facilitates the training, research and Consultancy projects by the Industries to the faculty.
- Organizes several collaborative programs as seminars, workshops, industry visits etc for the Students and Faculty.

Entuple Technologies Pvt., Ltd.:

Entuple is a next generation solutions enabler in cutting edge technologies. Head Quartered at Bangalore, India, Entuple delivers world class products & solutions in Applied Electromagnetics, Semiconductor and System Design & Reliability, Drivers & Power Systems, Telecom, Mechanical and Civil sector. We do offer R & D consulting across technologies. Our niche services include – IC fabrication alliance, Post silicon validation and more. We cater to wide range of customers in semiconductor, manufacturing, defense & aerospace and academia.

About the FDP/ Short Term Course:

VLSI technology has gone through rapid strides in last few decades. Despite digital processing of signals, advent of digital architecture and rapid growth of IC design technology, the basic abstraction layer for complex chipsets continuous to be Analog components. Analog circuit & layout design continuous to get more and more complex due to ever increasing demand for power, area and cost effective solutions in digital and analog IC design. Industry efforts are focused towards optimizing designs for better performance, area & energy and other key factors. Industry is looking at competent manpower to address these challenges on an ongoing basis. Academia is the main source of manpower to industry. Quality manpower from campuses is one of the key expectations of industry. Entuple believes in a philosophy of empowering faculty champions to groom competent future engineers of industry. The various learning activities driven by Entuple are focused towards this objective.

This Faculty Development Program (FDP) is designed to provide deeper aspects of Analog Circuit Design layout concepts. The program provides the industry ways of working environment for participants. It progressively builds the concepts with a kick start on functional blocks such as current mirrors, repeaters, operational amplifiers and delivers deep insights on characterization.

The program also caters to the needs of research scholars pursuing their research in custom IC Design/ Analog circuit and Layout. This program also benefits practicing engineers to fine tune their skill and work on analog circuit and layout design more effectively in their deliverables.

Key Learning Outcomes:

At the end of the program you will be able to:

- Analyze the performance specification requirements and identify the suitable circuit topologies
- Characterize the PDK for device analog model parameters
- Synthesize basic and OP-AMP amplifier circuit topologies
- Design CMOS Amplifier circuits for given DC and AC performance parameters
- Develop programmed spread sheets for amplifier design automation
- Design and characterize a seven – pack CMOS Compensated OP-AMP at the schematic design entry level
- Derive layout constraints for the physical design of the OP-AMP and carry out DRC and LVS
- Carry out the physical verification and parasitic

extraction.

- Back Annotate and carry out Post Layout Simulation/ Characterization

Who should attend?

- Practicing engineers in Analog circuit and layout design
- Faculty involved in teaching Analog CMOS IC Design and Analog Mixed Signal design courses
- Research scholars pursuing research in Analog circuit and Layout, device characterization and more.
- UG/PG students aspiring to get started with concepts of Analog circuit and layout foundation and planning for a career in semiconductor industry.

Course Outline and Structure

Day 1: Fundamentals of Standard Cell Modules - Design and Simulation of the balanced inverter, Layout Design Concepts

Session 1

1. Introduction to VLSI
2. CMOS inverter and its applications
   - Concept of balanced, symmetric and fastest inverter
   - Hands - on lab: Design and simulation of a CMOS inverter(gpdk180)
   - DC and Transient Analysis
   - Analysis of the quality metrics of designed inverter

Session 2

1. Custom IC design flow of designed balanced inverter
2. Hands - on Lab
   - Layout capture, Physical verification (DRC and LVS), Parasitic extraction (parasitic Resistance and Capacitance), Post Layout Simulation with parasitic back annotation, GDSII of the layout

Day 2: Digital ASIC Design

Session 1: Front End Design (Design Entry to Synthesis)

1. Introduction to ASIC design flow
2. CADENCE platform for digital design
   - Incisive, RTL Compiler, Encounter
3. Functional Simulation Using GUI
4. HDL Capturing and Functional Simulation of HDL codes - Basic gates, counter
5. Synthesis

Session 2: BACKEND DESIGN (RTL to GDSII)

1. Physical Design of counter HDL Design
   - Floor Planning, Power Planning, Placement,
   - CTS, Routing, Timing Analysis
2. GDSII & post layout files

Day3: Fundamentals of Analog Signal Processing – CMOS Amplifier Topologies and Performance

Session1:

1. Design and simulation of CS Amplifier with current source load: DC and small signal AC performance
2. Interpreting the Design Specifications

Session 2: Analog & mixed signal Design flow.

Registration Fee: **There is no Registration Fee**

For free Registration follow the link:

https://forms.gle/Ap2eE9cndqvVJz4J7

Lunch, Tea and Snacks will be provided for the participants at the Venue

Limited seats: Registration is on first come first serve basis. Selected participants will be informed by mail by **20th April, 2019.**.

Last date for registration: 20th April, 2019.

Travel/Accommodation

Participants are required to make their own arrangements for travel, local conveyance and accommodation.

Address for Correspondence

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Department of ECE, JNTUH CEH
Cell: 9848506611, Email: mlmakkena@yahoo.com

Venue: UIIC, JNTUH (Admissions Block),
Time: 10:00 AM to 5:00 PM

A Faculty Development Program on
"Analog IC Design- Hands on Practice using Cadence Design Flow"

22nd - 24th April, 2019

(Under TEQIP-III)

In collaboration with

ENTUPLE TECHNOLOGIES

Bangalore

Coordinators
Dr. Ch. Venkata Ramana Reddy
Director, UIIC, JNTUH

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