# M. Tech. (ES & VLSI) – R13 Regulations

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

*(Established by an Act No.30 of 2008 of A.P. State Legislature)*

Kukatpally, Hyderabad – 500 085, Andhra Pradesh (India)

M. Tech. (EMBEDDED SYSTEMS & VLSI DESIGN/VLSI AND EMBEDDED SYSTEMS)

## (R13) COURSE STRUCTURE AND SYLLABUS

### I Year - I Semester

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### I Year - II Semester

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M. Tech. (ES & VLSID/VLSI & ES) – R13 Regulations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech – I Year – I Sem. (ES & VLSID/VLSI & ES)

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT – I:
ARM Architecture:
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT – II:
ARM Programming Model – I:
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT – III:
ARM Programming Model – II:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions.

UNIT – IV:
ARM Programming:
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT – V:
Memory Management:

TEXT BOOKS:

REFERENCE BOOKS:
UNIT –I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} - V_{ds}$ relationships, Threshold Voltage $V_T$, $G_m$, $G_{ds}$ and $\omega_o$, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, $Z_{pu}/Z_{pd}$, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:
Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:
Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

REFERENCE BOOKS:
M. Tech. (ES & VLSID/VLSI & ES) –R13 Regulations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech – I Year – I Sem. (ES & VLSID/VLSI & ES)

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

UNIT I:
MOS Devices and Modeling:

UNIT II:
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III:
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV:
CMOS Operational Amplifiers:

UNIT V:
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

REFERENCE BOOKS:
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
UNIT-I:
Introduction to Programmable Logic Devices:

UNIT-II:
Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT-III:
SRAM Programmable FPGAs:

UNIT-IV:
Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:
Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
UNIT –I:
Co-Design Issues:
Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co-Synthesis Algorithms:
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:
Prototyping and Emulation:
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:
Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:
Design Specification and Verification:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:
Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
UNIT I:
Minimization and Transformation of Sequential Machines:
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

UNIT II:
Digital Design:
Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32-bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT III:
SM Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT IV:
Fault Modeling & Test Pattern Generation:
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models – Bridging fault model.

UNIT V:
Fault Diagnosis in Sequential Circuits:
Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:
M. Tech. (ES & VLSI/VLSID & ES) –R13 Regulations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (ES & VLSID/VLSI & ES)

SOFT COMPUTING TECHNIQUES
(ELECTIVE -I)

UNIT –I:
Introduction:
Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II:
Artificial Neural Networks:
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III:
Fuzzy Logic System:
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV:
Genetic Algorithm:
Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and ant-colony search techniques for solving optimization problems.

UNIT –V:
Applications:

TEXT BOOKS:

REFERENCE BOOKS:
ADVANCED OPERATING SYSTEMS (ELECTIVE -II)

UNIT –I:
Introduction to Operating Systems:
Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:
Introduction to UNIX and LINUX:
Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III:
System Calls:
System calls and related file structures, Input / Output, Process creation & termination.
Inter Process Communication:
Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:
Introduction to Distributed Systems:
Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed Systems:
Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:
Synchronization in Distributed Systems:
Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions
Deadlocks:
Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:
1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.

REFERENCE BOOKS:
UNIT –I:
Introduction:

UNIT –II:
Modern Techniques:
Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms:

Conventional Encryption:
Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography:
Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT –III:
Number Theory:
Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash Functions:
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT –IV:
Hash and Mac Algorithms:
MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication Protocols:
Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications:

UNIT –V:
IP Security:
Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security:

Intruders, Viruses and Worms:
Intruders, Viruses and Related threats.

Fire Walls:
Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

REFERENCES:
1. Principles of Network and Systems Administration, Mark Burgess, John Wiel
CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
(ELECTIVE – II)

UNIT – I:
MOS Design:
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage,
Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates,
Transistor equivalency, CMOS Inverter logic.

UNIT – II:
Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex
Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and
OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT – III:
Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge
triggered flipflop.

UNIT – IV:
Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS
transmission gate logic, High performance Dynamic CMOS circuits.

UNIT – V:
Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and
refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and
NAND flash.

TEXT BOOKS:
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC
   Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan,
   Borivoje Nikolic, 2nd Ed., PHI.
VLSI LABORATORY

Note:
- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:
Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Part –II: VLSI Back End Design programs:
Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - Basic logic gates
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS 1-bit full adder
   - Static / Dynamic logic circuit (register cell)
   - Latch
   - Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
EMBEDDED C

UNIT – I:
Programming Embedded Systems in C
Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family
Introduction, What’s in a name, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions

UNIT – II:
Reading Switches
Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III:
Adding Structure to the Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the ‘Hello Embedded World’ example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV:
Meeting Real-Time Constraints
Introduction, Creating ‘hardware delays’ using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for ‘timeout’ mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V:
Case Study: Intruder Alarm System
Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:
1. Embedded C by Michael J. Pont, A Pearson Education

REFERENCE BOOKS:
1. PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C By Nigel Gardner
CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT IV:
Nyquist Rate A/D Converters:

UNIT V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

REFERENCE BOOKS:
EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT – I:
Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O,( open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT - II:
Real Time Operating Systems

UNIT - III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
DESIGN FOR TESTABILITY

UNIT I:
Introduction to Testing:

UNIT II:
Logic and Fault Simulation:

UNIT III:
Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT IV:
Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT V:
Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

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JAWAHarlAL NEHRU TECHNOLoGICAL UNIVERSITY HYDRAbAD
M. Tech – I Year – II Sem. (ES & VLSID/VLSI & ES)

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE -III)

UNIT -I:
Introduction to Digital Signal Processing:
Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and Interpolation.

Computational Accuracy in DSP Implementations:
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT -II:
Architectures for Programmable DSP Devices:
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:
Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT -IV:
Analog Devices Family of DSP Devices:

UNIT -V:
Interfacing Memory and I/O Peripherals to Programmable DSP Devices:
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

REFERENCE BOOKS:
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
M. Tech (ES & VLSI/VLSI & ES) –R13 Regulations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (ES & VLSI/VLSI & ES)

SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -III)

UNIT –I:
Introduction to the System Approach:

UNIT –II:
Processors:

UNIT –III:
Memory Design for SOC:

UNIT –IV:
Interconnect Customization and Configuration:

UNIT –V:
Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

REFERENCE BOOKS:
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

EMBEDDED NETWORKING
(ELECTIVE -III)

UNIT –I:
Embedded Communication Protocols:

UNIT –II:
USB and CAN Bus:

UNIT –III:
Ethernet Basics:

UNIT –IV:
Embedded Ethernet:

UNIT –V:
Wireless Embedded Networking:

TEXT BOOKS:

REFERENCE BOOKS:
1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
SEN SORS AND ACT UTAORS
(ELECTIVE –IV)

UNIT -I:
Sensors / Transducers: Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization

UNIT –II:

UNIT -III:
Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistrs/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors

UNIT -IV:

UNIT -V:
Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators
Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection

TEXT BOOKS:

REFERENCE BOOKS:
LOW POWER VLSI DESIGN
(ELECTIVE -IV)

UNIT –I:
Fundamentals:

UNIT –II:
Low-Power Design Approaches:
Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:
Low-Voltage Low-Power Adders:

UNIT –IV:
Low-Voltage Low-Power Multipliers:
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:
Low-Voltage Low-Power Memories:

TEXT BOOKS:
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:
SEMICONDUCTOR MEMORY DESIGN AND TESTING
(ELECTIVE -IV)

UNIT -I:
Random Access Memory Technologies:
SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT -II:
Non-volatile Memories:
Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III:
Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV:
Semiconductor Memory Reliability and Radiation Effects:
General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V:
Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:
EMBEDDED SYSTEMS LABORATORY

Note:
- The following programs are to be implemented on ARM based Processors/Equivalent.
- Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

Part -I:
The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

Part -II:
Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
   b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:
6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.