# M.TECH. (DIGITAL SYSTEMS & COMPUTER ELECTRONICS) (R13) COURSE STRUCTURE AND SYLLABUS

## I Year - I Semester

<table>
<thead>
<tr>
<th>Code</th>
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## I Year - II Semester

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## II Year - I Semester

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UNIT –I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} - V_{ds}$ relationships, Threshold Voltage $V_T$, $G_m$, $G_{ds}$ and $\omega_o$. Pass Transistor, MOS, CMOS & BiCMOS Inverters, $Z_{pu}/Z_{pd}$. MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:
Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:
Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

REFERENCE BOOKS:
UNIT - I:
Minimization and Transformation of Sequential Machines:
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

UNIT - II:
Digital Design:
Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT - III:
SM Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT - IV:
Fault Modeling & Test Pattern Generation:
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

UNIT - V:
Fault Diagnosis in Sequential Circuits:
Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:
UNIT -I:
Digital Modulation Schemes:
BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT -II:
Basic Concepts of Data Communications, Interfaces and Modems:

UNIT -III:
Error Correction: Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code
Data Link Control: Line Discipline, Flow Control, Error Control

UNIT -IV:
Multiplexing: Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, DSL
Local Area Networks: Ethernet, Other Ether Networks, Token Bus, Token Ring, FDDI.
Metropolitan Area Networks: IEEE 802.6, SMDS
Switching: Circuit Switching, Packet Switching, Message Switching.
Networking and Interfacing Devices: Repeaters, Bridges, Routers, Gateway, Other Devices.

UNIT -V:
Multiple Access Techniques:
Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization, Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code- Division Multiple Access (CDMA), OFDM and OFDMA.

TEXT BOOKS:

REFERENCE BOOKS:
1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT –I:
ARM Architecture:
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:
ARM Programming Model – I:
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:
ARM Programming Model – II:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions.

UNIT –IV:
ARM Programming:
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:
Memory Management:

TEXT BOOKS:

REFERENCE BOOKS:
UNIT I:
MOS Devices and Modeling:

UNIT II:
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III:
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV:
CMOS Operational Amplifiers:

UNIT V:
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

REFERENCE BOOKS:
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
IMAGE AND VIDEO PROCESSING
(ELECTIVE -I)

UNIT –I:
Fundamentals of Image Processing and Image Transforms:
Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation:
Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II:
Image Enhancement:
Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT –III:
Image Compression:
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, , Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT –IV:
Basic Steps of Video Processing:

UNIT –V:
2-D Motion Estimation:
Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

REFERENCE BOOKS:
EMBEDDED SYSTEMS DESIGN
(ELECTIVE – I)

UNIT -I:
Introduction to Embedded Systems:

UNIT -II:
Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III:
Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV:
RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V:
Task Communication:
Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:
1. Embedded Systems - Raj Kamal, TMH.
4. An Embedded Software Primer - David E. Simon, Pearson Education.
UNIT –I:
MOS Design:
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:
Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OI gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:
Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:
Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:
Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

REFERENCE BOOKS:
INTERNETWORKING
(EIFECTIVE - II)

UNIT -I:
Internetworking Concepts:

IP Address:
Classful Addressing:
Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting

Classless Addressing:

ARP and RARP: ARP, ARP Package, RARP.

UNIT -II:
Transmission Control Protocol (TCP):
TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.

Stream Control Transmission Protocol (SCTP):
SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Classical TCP Improvements:
Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

UNIT -III:
Unicast Routing Protocols (RIP, OSPF, and BGP):
Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.

Multicasting and Multicast Routing Protocols:
Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

UNIT -IV:
Domain Name System (DNS):
Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.

Remote Login TELNET: Concept, Network Virtual Terminal (NVT).

File Transfer FTP and TFTP:
File Transfer Protocol (FTP).

Electronic Mail: SMTP and POP.

Network Management-SNMP:

UNIT -V:
Multimedia:

TEXT BOOKS:
2. Internetworking with TCP/IP Comer 3rd Edition PHI

REFERENCE BOOKS:
UNIT –I: 
Introduction:
Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II: 
Artificial Neural Networks:
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III: 
Fuzzy Logic System:
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV: 
Genetic Algorithm:
Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and ant-colony search techniques for solving optimization problems.

UNIT –V: 
Applications:

TEXT BOOKS:

REFERENCE BOOKS:
SIMULATION LAB

Note:
A. Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:
Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

Part –II: VLSI Back End Design programs:
Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - Basic logic gates
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS 1-bit full adder
   - Static / Dynamic logic circuit (register cell)
   - Latch
   - Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
ADVANCED COMPUTER ARCHITECTURE

UNIT I:
Fundamentals of Computer Design:
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl’s law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT II:
Pipelines:
Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design:

UNIT III:
Instruction Level Parallelism (ILP) - The Hardware Approach:
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, High performance instruction delivery- Hardware based speculation.
ILP Software Approach:
Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware versus Software.

UNIT IV:
Multi Processors and Thread Level Parallelism:
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT V:
Inter Connection and Networks:
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture:
Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

REFERENCE BOOKS:
LOW POWER VLSI DESIGN

UNIT –I:
Fundamentals:

UNIT –II:
Low-Power Design Approaches:
Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:
Low-Voltage Low-Power Adders:

UNIT –IV:
Low-Voltage Low-Power Multipliers:
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:
Low-Voltage Low-Power Memories:

TEXT BOOKS:
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:
DESIGN FOR TESTABILITY

UNIT -I:
Introduction to Testing:

UNIT -II:
Logic and Fault Simulation:

UNIT -III:
Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:
Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:
Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

REFERENCE BOOKS:
EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT – I:
Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT – II:
Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT – III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT – IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT – V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS and Basic Concepts of Android OS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
UNIT-I:
Introduction to Programmable Logic Devices:

UNIT-II:
Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:
SRAM Programmable FPGAs:

UNIT -IV:
Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:
Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
M.TECH. (DIGITAL SYSTEMS & COMPUTER ELECTRONICS)-R13 Regulations
JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech – I Year – II Sem. (DSCE)

NETWORK SECURITY AND CRYPTOGRAPHY
(ELECTIVE -III)

UNIT –I:
Introduction:

UNIT –II:
Modern Techniques:
Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
Algorithms:

Conventional Encryption:
Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography:
Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT –III:
Number Theory:
Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.
Message authentication and Hash Functions:
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT –IV:
Hash and Mac Algorithms:
MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication Protocols:
Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications:

UNIT –V:
IP Security:
Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security:

Intruders, Viruses and Worms:
Intruders, Viruses and Related threats.

Fire Walls:
Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

REFERENCE BOOKS:
1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
5. Introduction to Cryptography, Buchmann, Springer.
UNIT –I:
Introduction to the System Approach:

UNIT –II:
Processors:
Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling, Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:
Memory Design for SOC:

UNIT –IV:
Interconnect Customization and Configuration:

UNIT –V:
Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

REFERENCE BOOKS:
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
UNIT I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT IV:
Nyquist Rate A/D Converters:

UNIT V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

REFERENCE BOOKS:
UNIT –I:
Introduction to Digital Signal Processing:
Introduction, a Digital signal-processing system, the sampling process, discrete time sequences.
Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems,
Digital filters, Decimation and interpolation.
Computational Accuracy in DSP Implementations:
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:
Architectures for Programmable DSP Devices:
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT –III:
Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs,
Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:
Analog Devices Family of DSP Devices:
Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:
Interfacing Memory and I/O Peripherals to Programmable DSP Devices:
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

REFERENCE BOOKS:
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
TCP/IP AND ATM NETWORKS
(ELECTIVE -IV)

UNIT –I:
Internet Protocol:
Internetworking, IPV4, IPV6, Transition from IPV4 to Ipv6.Process to process delivery, UDP, TCP and SCTP.

UNIT –II:
Congestion Control and Quality of Service:
Data traffic, congestion, congestion control, two examples, Quality of Service, Techniques to improve QOS, Integrated services, and Differentiated services.

UNIT –III:
Spread Spectrum:
Introduction, Basic Concept, Protection against Jamming, Spreading Codes (PN-Sequence), Generation, Properties, Types of Spread Spectrum Techniques, Application Of Spread Spectrum.

UNIT –IV:

UNIT –V:
Interconnection Networks:
Introduction, Banyan Networks, Properties, Crossbar Switch, Three Stage Class Networks, Rearrangeble Networks, Folding Algorithm ,Benes Networks, Lopping Algorithm, Bit Allocation Algorithm.
SONET/SDH:-Synchronous Transport Signals, Physical Configuration, SONET Layers, SONET Frame.

TEXT BOOKS:

REFERENCE BOOKS:
2. Wireless Digital Communications –Kamil Feher-1999 PHI
EMBEDDED SYSTEMS LABORATORY

Note:
- The following programs are to be implemented on ARM based Processors/Equivalent.
- Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

Part -I:
The following Programs are to be implemented on ARM Processor
1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

Part -II:
Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:
1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
   4. a).Write an application to Test message queues and memory blocks.
      b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:
6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.